CAL LAB
W-97

WAVETEK®

OPERATOR'S & MAINTENANCE MANUAL

Model 178

50 MHz Programmable Waveform Synthesizer

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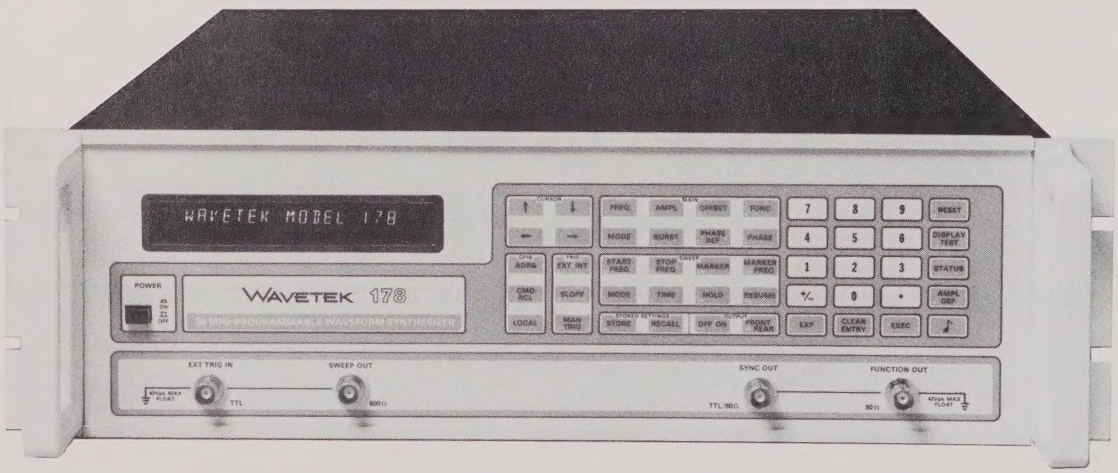
SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.



Model 178, 50 MHz Programmable Waveform Synthesizer

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 178

The Model 178 Programmable Waveform Synthesizer is a 1 μHz to 50 MHz multifunction sweep synthesizer that can operate as a trigger, gate or burst generator at levels to 20 volts peak-to-peak. It is synthesized to 8 digits in all modes.

Its main generator, an 8 digit 50 MHz synthesizer, produces sine and square waves and, at reduced frequencies, triangles, ramps, pulses and haverwaves.

An external reference input can phase lock the synthesizer by locking the reference source. Phase locking allows the synthesizer to operate as a variphase generator with phase offset in 0.01° increments.

The output level is specified into a 50Ω load from 1 mV to 20 Vp-p with 3 digits resolution. DC offset can be programmed to vary the waveform base line ±10V. Amplitude is displayed in units of Vp-p, Vrms or dBm for any waveform.

The internal sweep generator varies the main generator frequency (linearly or logarithmically) between the start and stop frequencies. The sweep generator has its own operating modes: triggered, gated, hold at start and hold at stop. In addition, ten programmable frequency markers, available one at a time, can be used to indicate critical frequencies within the sweep. The sweep generator can internally trigger the main generator to produce pulses with a 10 μs to 10 min. repetition rate and 5 μs to 5 days pulse width.

Two external inputs may be used to phase- or amplitude-modulate the synthesizer. If the synthesizer is phase modulated, the main generator (when operating at frequencies above 500 kHz) varies up to ±360°. When amplitude modulated, the output can be modulated up to 200%.

Data entry is from the front panel or GPIB with microprocessors controlling the data. Numeric input is entered in free format: fixed, floating or exponential notation. Parameters may be entered in any order. Internally, all entries are checked for errors and interactively displayed on the front panel.

Up to 5 complete sets of programming may be stored and rapidly recalled.

1.2 OPTIONS

Option 001 allows up to 40 sets of complete front panel settings to be stored in memory. Memory is battery backed up (internally recharged) for 60 days (minimum) retention of settings. Memory is expandable to 240 settings.

Option 002 provides an additional high stability frequency reference crystal for greater accuracy. The high stability frequency has an accuracy of $\pm 5 \times 10^{-8}$ and an aging rate of 5×10^{-9}/day (average) or $<4 \times 10^{-8}$/week

1.3 SPECIFICATIONS

1.3.1 Versatility

Waveforms

Sine ∿ , square ⊓ , triangle △ , ramps ◿, ◺, haversine ⩚ , ⩛ , havertriangles ⩚ , ⩛ , AM (sine) ◇◇ , and DC.

Operational Modes

NOTE

1. *All modes are synthesized.*
2. *See Frequency Range Section for frequency capability in each mode.*
3. *Trigger modes: Trigger jitter <1% of waveform period.*

Continuous: Generator runs continuously.

Triggered: Generator is quiescent until triggered by an external signal, internal sweep signal, GPIB or manual trigger, then generates one cycle at selected frequency.

Gated: As triggered mode, except generator oscillates for the duration of the gate signal plus the remainder of the waveform in progress.

Triggered Haverwave: As triggered mode, except output is a sine or triangle waveform starting at −90° (or +90°).

Gated Haverwave: As gated mode, except output is a sine or triangle waveform starting at −90° (or +90°).

Triggered Burst: As triggered mode, except the number of cycles output for each trigger input is selectable from 1 to 65,536 (2^{16}) counts.

Triggered Haverwave Burst: As triggered burst, except output is a sine or triangle waveform starting at −90° (or +90°).

Frequency Sweep: Output frequency can be swept by internal sweep generator. (See Sweep Generator).

Frequency Range
Low-end frequency for all waveforms is 1μHz.

Continuous Mode:
∿ , ⊓ , ◇◇ (AM sine) to 50 MHz.
∿ to 500 kHz.
⟋, ⟍ to 20 kHz.

All Triggered Gated and Burst Modes:
∿ , ⊓ , ∿ , ◇◇ (AM sine) to 200 kHz.
⟋, ⟍ to 20 kHz.

Main Output
All waveforms are available to 20 Vp-p maximum into 50Ω load. Combined amplitude/dc offset waveforms not to exceed ±10V peak into 50Ω. Output voltage into an open circuit is double indicated voltage when a voltage less than ±5V peak is selected. Output available from front or rear. Source impedance: 50Ω (for <10V output), hi Z (for >10V output). Output may be floated up to 42V peak.

Phase Offset: Output phase may be changed from ±1000 revolutions (±360,000°) in 0.01° resolution steps to 500 kHz and 0.1° (or better) resolution steps above 500 kHz.

Amplitude Conversion
Permits entry and display of amplitude for all waveforms in units of Vrms, Vp-p and dBm.

DC Offset and DC Voltage Output
0 to ±10 Vdc into 50Ω. Output voltage is double into open circuit when voltage less than ±5 Vdc is selected.

Auxiliary Outputs
TTL and TTL Sync: At generator frequency, 50Ω source impedance, 50% duty cycle, <5 ns transition time.

Reference Output: 10 MHz, 1 Vp-p sine, 50Ω source impedance.

Sweep Ramp: (See Sweep Generator).

Frequency Marker: (See Sweep Generator).

Inputs
Trigger: A TTL level transition can trigger or gate both main generator and/or internal sweep generator. Triggering slope up (⌐) or down (¬) is selectable.

Reference: An external 0.5V to 10 Vp-p sine or pulse clock of ±5 ppm or better stability and accuracy automatically locks the internal reference. External clock may be 1, 2, 3..., 9 or 10 MHz. Input impedance is 1 kΩ.

Amplitude Modulation: Modulation levels up to 20 kHz. Input impedance is 600 ohms. Amplitude reduced by approximately 50% with 0V input. 5.4 Vp-p, ±15%, ac signal (with 0V offset) provides 99% modulation. AC signal with −2.7 Vdc, ±15%, provides 200% modulation. Modulation bandwidth typically 10 MHz. Sync output unaffected by modulation.

Phase Modulation: Rates from DC to 10 kHz minimum. Input impedance is 10 kΩ. ±5V input delivers approximately ±360° shift. Output deviation is ÷100 for main output frequencies 500 kHz and below.

Data Entry
Front panel keyboard with display and GPIB programming.

1.3.2 Main Generator

1.3.2.1 Frequency Resolution

8 digits or 1μHz.

1.3.2.2 Frequency Precision

Accuracy

Better than 0.0005% of program setting, ±0.01 μHz.

Stability
Long Term: $\pm 1 \times 10^{-6}$/mo.

Temperature: $\pm 1.2 \times 10^{-7}$/°C.

Signal to Phase-Noise
Better than −46 dB in a 30 kHz band centered on carrier but excluding a ±1 Hz band around the carrier.

Spurious

-60 dBc or 30 μV whichever is greater, 1 μHz to 200 kHz.
-54 dBc or 30 μV whichever is greater, >200 kHz to 500 kHz.
-44 dBc or 30 μV whichever is greater, >500 kHz to 50 MHz.

1.3.2.3 Amplitude Precision

Resolution and Accuracy

NOTE
DC offset range is 0 to ± 10 Vdc

Amplitude Range	Accuracy (Amplitude)
10.02 to 20.00 Vp-p	±1% ±20 mV
1.01 to 10.0 Vp-p	±1% ±10 mV
0.101 to 1.00 Vp-p	±3% ±2 mV
10.1 to 100 mVp-p	±4% ±100 µV
1.00 to 10.0 mVp-p	±5% ±20 µV

NOTE
Specified for 1 kHz sine wave, or for dc output into a precision 0.1% 50Ω load.

Resolution: 3 digit ≤10.0 Vp-p, 4 digit (20 mV) >10 Vp-p.
DC Offset: ±1% of setting ±40 mV (worst case).

NOTE
Amplitude and dc offset share the output attenuator.

Frequency Response

Frequency Range	Response
1 µHz to 20 kHz	±1%
>20 kHz to 500 kHz	±3%
>500 kHz to 25 MHz	±7%
>25 MHz to 50 MHz	±15%

Specified relative to 1kHz sine wave, >100 mV to 6Vp-p, 0V offset into 50Ω.

Frequency Range	Response
1 µHz to 20 kHz	±1%
>20 kHz to 500 kHz	±3%
>500 kHz to 7 MHz	±7%
>7 MHz to 20 MHz	±12%
>20 MHz to 50 MHz	±20%

Specified relative to 1 kHz sine wave, >6V to 10 Vp-p, 0V offset into 50Ω.

For square add 1%. For triangle add 1% to 20 kHz; for greater than 20 kHz, unspecified.

For ramps add 5% to 10 kHz; add 15% to 20 kHz.

Amplitude and Offset Stability
Short Term: 0.1% ±1 mV for 10 min.
Long Term: 0.5% ±5 mV for 6 months.
Measured at room temperature.

1.3.2.4 Waveform Characteristics

Sine Distortion
Harmonically related signals less than:
–55 dB to 50 kHz.
–40 dB to 500 kHz.
–30 dB to 50 MHz.
Specified for 1 Vrms (2.83 Vp-p) sine wave.

Square Wave Rise and Fall Time
Less than 10 ns, 1.01 to 10.00 Vp-p
Less than 12 ns, greater than 10 Vp-p

Square Wave Aberrations
≤5% ± 50 mV of p-p voltage

1.3.3 Sweep Generator

Sweep generator is fully synthesized and may be used independently or for frequency sweeping and triggering the main generator. Frequency sweep may be selected linear or logarithmic, and up or down. Sweep may be triggered, interrupted with hold, and continued with resume.

1.3.3.1 Sweep Modes

Continuous Sweep: Sweep generator sawtooth runs continuously

Triggered Sweep: Incoming trigger causes a single sweep and resets to the start frequency.

Triggered Sweep/Triggered Reset: As in triggered sweep, but sweep holds at stop frequency until subsequent trigger returns frequency to start frequency.

1.3.3.2 Sweep Characteristics

Sweep Time
0.01 to 600.00 sec, 10µs resolution.

Sweep Output
0 to approximately +5V ramp synthesized to 2000 steps per sweep. 600Ω output impedance.

Frequency Marker Output
TTL levels. One of the ten preset markers can be selected. Output is low when the main generator frequency is below marker frequency; output is high when above. Crystal clock accuracy equal to that of synthesizer.

Maximum Sweep Range
Low Band: 1 µHz to 500 kHz.
High Band: 5 kHz to 50 MHz.

Minimum Sweep Range

Linear: Any start and stop frequencies with a minimum separation of:

Low Band: 20 mHz per 1s of sweep time.
High Band: 2 Hz per 1s of sweep time.

Log: Any start and stop frequencies with ratio greater than 2.

Sweep Resolution
Frequency Resolution including Start, Stop, Hold, Markers: 8 digits or 1 μHz.

Sweep Frequency Update: Every 5 μs (lin and log).

Log Slope Update: Every 2 ms.

1.3.3.3 Pulses
Square function triggered by sweep generator. Pulse parameters of period and width are controlled by sweep time and main generator frequency respectively. Pulses are generated to high synthesizer resolution and accuracy. Pulse is continuous or triggered externally.

Period
10 μs to 600s.
4 digits or 10 μs resolution (Control: Sweep Time); jitter <2% of pulse width.

Width
5 μs to 500,000s (>5 days);
8 digits resolution (Control: Main Frequency);
<0.05% jitter.

NOTE
Width is usable to 1 μs.

1.3.4 General

Stored Settings
Up to 5 complete instrument setups can be stored and recalled from volatile (RAM) memory. Settings may be modified or deleted.

GPIB Programming
Standard General Purpose Interface Bus (GPIB) programming per IEEE Standard 488-1978. Interface is optically isolated from signal ground. Interface includes Listener (AH1 and L4), Talker (SH1 and T6), SRQ (SR1), Local Lockout (RL1), Device Clear (DC1), Group Execute Trigger (DT1) capabilities, and open collector logic (E2).

Parameter	Time
Command Handshake	15 μs
Data Handshake	65 μs
Frequency	11 ms
Amplitude	14 ms
DC Offset	14 ms
Mode	4 ms
Function	5 ms
Output	4 ms
Stored Settings	13 ms
Execute	8 ms

NOTE
Above programming speeds are typical. Programming times vary with different controllers. Data rate follows slowest listener on bus.

Environmental
Accuracy applies for 25°C ±10°C after 30 minutes warm-up unless otherwise noted. Instrument will operate from 0°C to 50°C to 10,000 ft altitude at 90% relative humidity. Storage temperature from −25°C to +65°C.

Dimensions
44.5 cm (17.5 in.) wide; 13.3 cm (5¼ in.) high; 53.4 cm (21 in.) deep. Supplied with rack mount adapters.

Weight
13.6 kg (30 lb) net; 19.4 kg (43 lb) shipping.

Power
90 to 105V, 108 to 126V, 198 to 231V or 216 to 252V; 48 to 67 Hz; less than 180 watts.

1.3.5 Options

001 Additional Stored Settings
Provides nonvolatile memory for 240 additional stored settings. Memory is battery backed up (internally recharged) for 60 day (minimum) retention of settings.

002 High Stability Frequency Reference

An additional frequency reference crystal for greater accuracy.

Accuracy: $\pm 5 \text{ X-}10^{-8}$
Aging Rate: $5 \text{ X } 10^{-9}$/day (average) $< 4 \text{ X } 10^{8}$/week.

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

CAUTION

Do not mount this instrument by front panel alone. Slides or tray support is necessary to prevent instrument damage. (Ref: Figure 2-1.)

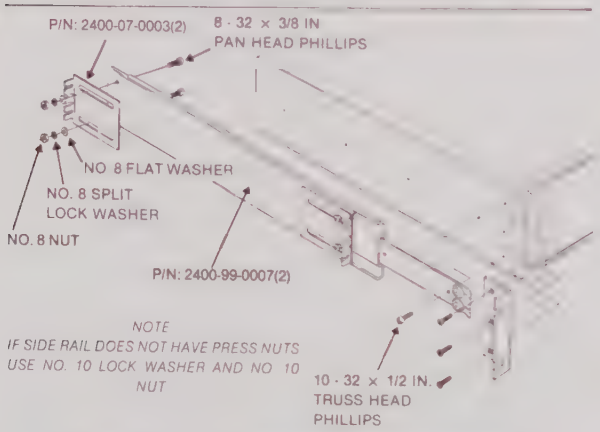

P/N: 2400-07-0003(2)
8 - 32 x 3/8 IN PAN HEAD PHILLIPS
NO. 8 FLAT WASHER
NO. 8 SPLIT LOCK WASHER
NO. 8 NUT
P/N: 2400-99-0007(2)
NOTE
IF SIDE RAIL DOES NOT HAVE PRESS NUTS USE NO. 10 LOCK WASHER AND NO 10 NUT
10 - 32 x 1/2 IN. TRUSS HEAD PHILLIPS

Figure 2-1. Optional Slide Mounting

The generator can be used as a bench instrument or rack mounted. In either use, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 2.2.5) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 2 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1A) according to the following procedure.

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90 to 105	2 amp
120	108 to 126	2 amp
220	198 to 231	1 amp
240	216 to 252	1 amp

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

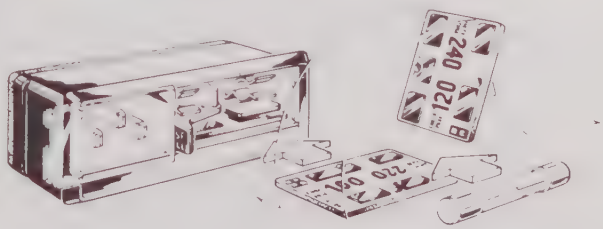


Figure 2-1A. Voltage Selector and Fuse

2.2.2 Signal Connections

NOTE

Use RG58U or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute FUNCTION OUT signals.

Instrument BNC connectors are:

EXT TRIG IN, front and rear panel, TTL

SWEEP OUT, front panel, 0 to ≈5V, 600Ω impedance.

SYNC OUT, front panel, TTL, 50Ω impedance

SYNC OUT, rear panel, $\overline{\text{TTL}}$, 50Ω impedance

FUNCTION OUT, front and rear panel, 10 Vp-p, 50Ω impedance; 10 to 20 Vp-p, >10 kΩ impedance.

REF IN, rear panel, 0.5V to 10 Vp-p, 1 to 10 MHz

REF OUT, rear panel, 10 MHz, 2 Vp-p, 50Ω impedance

MARKER OUT, rear panel, TTL

AM IN, rear panel 5 Vp-p (100% modulation), 600Ω impedance

ϕ MOD IN, rear panel, 5 Vp-p Maximum, 10 kΩ impedance

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Chassis Ground	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Ground
19		
20		
21		
22		
23		
24		

Signal ground may be floated up to ±42 volts with respect to chassis ground. Be aware that if one signal ground is floated, all signal grounds, on both front and rear panels, are likewise affected.

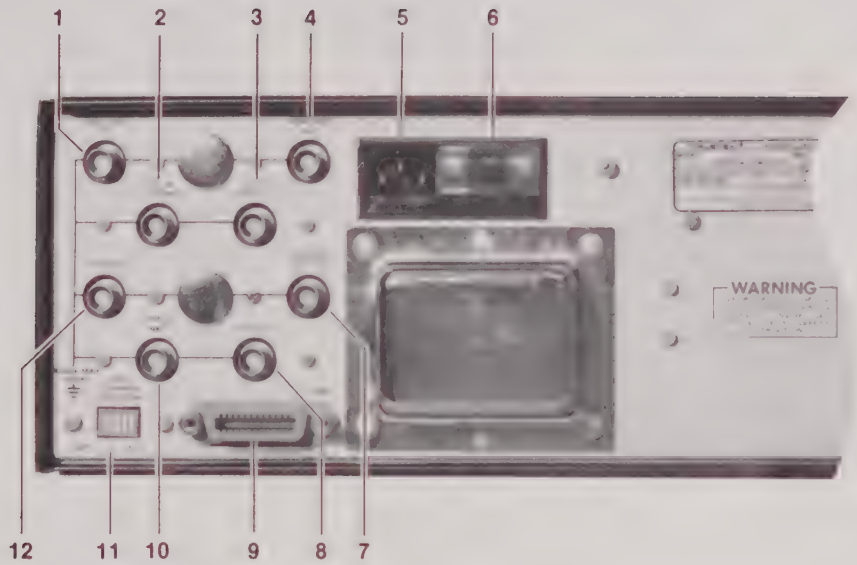
2.2.3 GPIB Connections

The GPIB I/O rear panel connection is shown in figure 2-2; pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths). The GPIB interface is optically isolated from the main generator.

Table 2-2. GPIB Address Codes

Device	ASCII		Switch Position					Hexa-decimal	
	Listen	Talk	1	2	3	4	5	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	1	0	0	0	0	21	41
2	"	B	0	1	0	0	0	22	42
3	#	C	1	1	0	0	0	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	1	0	1	0	0	25	45
6	&	F	0	1	1	0	0	26	46
7	'	G	1	1	1	0	0	27	47
8	(	H	0	0	0	1	0	28	48
9	)	I	1	0	0	1	0	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	1	1	0	1	0	2B	4B
12	,	L	0	0	1	1	0	2C	4C
13	—	M	1	0	1	1	0	2D	4D
14	•	N	0	1	1	1	0	2E	4E
15	/	O	1	1	1	1	0	2F	4F
16	0	P	0	0	0	0	1	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	0	1	0	0	1	32	52
19	3	S	1	1	0	0	1	33	53
20	4	T	0	0	1	0	1	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	0	1	1	0	1	36	56
23	7	W	1	1	1	0	1	37	57
24	8	X	0	0	0	1	1	38	58
25	9	Y	1	0	0	1	1	39	59
26	:	Z	0	1	0	1	1	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	0	0	1	1	1	3C	5C
29	=	]	1	0	1	1	1	3D	5D
30	>	↑	0	1	1	1	1	3E	5E

Address 31 is not allowed.



Location	Function	Paragraph
1	Function Output	2.2.2, 3.11, App E
2	Reference Input	2.2.2, 3.8.6
3	Reference Output	2.2.2, 3.8.6
4	Sync Output	2.2.2
5	Power Cord Receptacle	2.2.1
6	Fuse and Fuse Holder	2.2.1
7	Marker Output	2.2.2, 3.9.6
8	Phase Modulation Input	2.2.2, 3.8.6
9	GPIB (General Purpose Interface Bus) Connector	2.2.3, 3.16
10	AM Input	2.2.2, 3.8.4
11	GPIB Address Selector Switch	2.2.4
12	Trigger Input	2.2.2, 3.7

Figure 2.2 Rear Panel and Cross Reference

2.2.4 GPIB Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the GPIB address is correct. The GPIB address can be changed by the switch on the rear of the instrument (see figure 2-2) by simply setting the multiple section switch located on the rear panel according to table 2-2. The switch sections are labeled from 1 through 5 and their open position noted (OPEN = Binary "0" in table 2-2). To verify the address, press ADR on the front panel. The device number (decimal) and ASCII listen and talk addresses will be displayed.

2.2.5 Initial Checkout and Operation

Make the equipment setup as shown in figure 2-3 and perform the steps in table 2-3 to verify Model 178 operation. If further explanations are required, refer to figure 3-1 and table 3-1.

Table 2-3. Operation Verification

Step	Test	Tester & Setup	Program	Desired Results
1	Wake-up state and Self Test	Connect Model 178 and oscilloscope as shown in figure 2-3. Scope setting: CH1 0.5 V/div, CH2 0.1 V/div, select CH1 only, horizontal 0.2 ms/div, trigger to external	Power: ON	Display: All segments, decimal points and commas light up for one second TYPICAL OF 20, SELF-TEST for one second, then WAVETEK MODEL 178. Scope: CH1 1 kHz, 1 Vp-p sine wave.
2		Select CH2		CH2, sweep signal 0 to ≥ +200 mV, 2s per sweep.
3	Wake-up Status		Press STATUS key	Display (changes automatically): FREQ 1 kHZ AMPL 1 V P-P OFFSET 0 V FUNC SINE (0) MODE CONTINUOUS (0) BURST COUNT 2 PHASE 0 DEG SW STRT 500 HZ SW STOP 5 kHZ MKR FRQ 1 kHz SWP OFF (0) SWEEP TIME 2 SEC OUTPUT ON (1) FRONT OUTPUT (0) EXTERNAL TRIGGER (0) TRIG SLOPE POS (0)

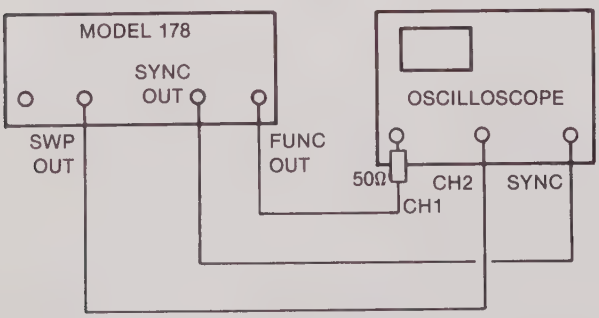


Figure 2-3. Step 1 Setup

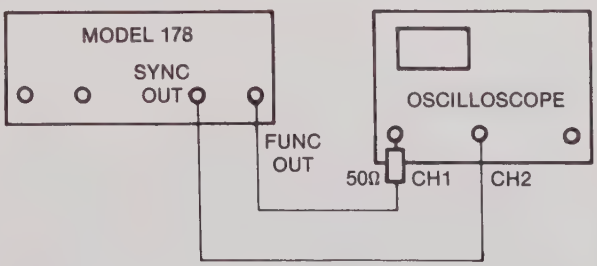


Figure 2-4. Step 59 Setup

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
4	Status Search		STATUS	Status display sequence stops.
5			↑	Status progresses forward.
6			↓	Status progresses backward.
7			STATUS	Status display sequentially continues.
8	Display Test		DISPLAY TEST	All segments decimal points, and commas light up. Back to last display when released.
9			Press FREQ key a few times	Beeper sounds everytime key is pressed.
10			Press ♪, then FREQ key a few times	Beeper is silent.
11			♪	Beeper enabled.
12	Command Recall		Press each of the 8 keys in the MAIN generator section 4 times then CMD RCL	Strings of characters shown on display.
13			Press ← or →	Moves characters left or right, 4 at a time.
14	GPIB Address and Status		ADRS	Display: GPIB ADDR ____ (Ref: Table 2-2)
15	Set Frequency		FREQ	Display: FREQ 1 kHZ.
16			←	Display: FREQ 1.0000000 kHZ.
17			↑	Frequency LSD increases.
18			↓	Frequency LSD decreases.
19			←or→	Different digits are intensified (selected for editing).
20	Reset Frequency	Select CH1	←or→ until digit selection (intensification) stops.	Display: FREQ 1 KHZ Scope: 1 kHz, 1 Vp-p sine wave.
21	Set Amplitude		AMPL	Display: AMPL 1 V P-P
22			Use cursor, ← → ↑ ↓, to increase or decrease amplitude	Scope: Amplitude increasing or decreasing.
23	Amplitude	Scope setting: 5 V/div	AMPL 20 EXEC	Scope: Sine wave 20 Vp-p. Display: AMPL 20 VP-P

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
24		2 V/div	AMPL 10 EXEC	Scope: 10 Vp-p
25		20 mV/div	AMPL .1 EXEC	Scope: 100 mVp-p
26		5 mV/div	AMPL 1 EXP – 2 EXEC	Scope: 10 mVp-p
27		5 mV/div	AMPL 1 EXP – 3 EXEC	Scope: 1 mVp-p
28		0.5 V/div	AMPL 1 EXEC	Scope: 1 Vp-p
29	Offset	Scope setting: 1 V/div	OFFSET 2 EXEC	Scope: 1 Vp-p sine wave, + 2 Vdc offset.
30			OFFSET – 2 EXEC	– 2 Vdc offset.
31			Use cursor to increase or decrease offset	Offset increases or decreases.
32			OFFSET 0 EXEC	1 Vp-p sine wave, 0 Vdc offset.
33	Function (Waveform, Low Frequency)	Scope setting: 0.2 V/div	FUNC	Display: FUNC SINE (0). Scope: 1 Vp-p, sine wave.
34			↑	Display: FUNC TRIANGLE (1). Scope: 1 Vp-p triangle wave.
35			↑	Display: FUNC SQUARE (2). Scope: 1 Vp-p square wave.
36			↑	Display: FUNC RAMP (3). Scope: 1 Vp-p ramp.
37			↑	Display: FUNC DC (4). Scope: 0 Vdc.
38			↑	Display: FUNC AM SINE (5). Scope: 0.5 Vp-p, sine wave.
39	Function (Waveform, High Frequency)	Scope setting: Horizontal 50 ns/div	FUNC 0 FREQ 1 EXP 7 EXEC	Display: FREQ 10 MHz Scope: 10 MHz, 1 Vp-p sine wave.
40			FUNC 2 EXEC	Display: FUNC SQUARE (2). Scope: 10 MHz, 1 Vp-p square wave.
41		Scope setting: Vert 2V/div, Horiz 10 ns/div	AMPL 10 FREQ 5 EXP 7 EXEC	Display: FREQ 50 MHz. Scope: 50 MHz, approx 8 Vp-p square wave.
		NOTE: Quality of waveform is dependent on cable length and speed of scope.		
42	System Reset (Reset to wake-up state)	Scope setting: Horizontal 0.5 ms/div CH1 0.5 V/div	RESET	Display: RESET. Scope: 1 kHz, 1 Vp-p sine wave.
43	Amplitude Definition		AMPL	Display: AMPL 1 V P-P
44			AMPL DEF	Display: AMPL IN VP-P (0).

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
45			↑	Display: AMPL IN VRMS (1)
46			AMPL	Display: AMPL 354 mV RMS.
47			FUNC 1 EXEC AMPL	Display: AMPL 289 mV RMS. Scope: 1 Vp-p triangle.
48			FUNC 2 EXEC AMPL	Display: AMPL 500 mV VRMS. Scope: 1 Vp-p square wave.
49			FUNC 0 AMPL 1 EXEC	Display: AMPL 1 V RMS. Scope: 2.83 Vp-p, sine wave.
50			FUNC 1 EXEC AMPL	Display: AMPL 1 V RMS. Scope: 3.46 Vp-p, triangle wave.
51			FUNC 2 EXEC AMPL	Display: AMPL 1 V RMS. Scope: 2 Vp-p square wave.
52			FUNC 3 EXEC AMPL	Display: AMPL 1 V RMS. Scope: 3.46 Vp-p, ramp.
53			AMPL DEF 2 EXEC	Display: AMPL IN dBm (2).
54			AMPL	Display: AMPL 13 dBm. Scope: 3.46 Vp-p ramp.
55			FUNC 2 EXEC AMPL	Display: AMPL 13 dBm. Scope: 2 Vp-p square wave.
56			FUNC 1 EXEC AMPL	Display: AMPL 13 dBm. Scope: 3.46 Vp-p triangle wave.
57			FUNC 0 EXEC AMPL	Display: AMPL 13 dBm. Scope: 2.83 Vp-p sine wave.
58	System reset		RESET	Display: RESET. Scope: 1 kHz, 1 Vp-p sine wave.
59	Triggered	Attach scope per figure 2-4. Scope: CH1 0.5 V/div CH2 1 V/div Horizontal 2 ms/div Trigger to CH2	EXT/INT 1 TIME .01 MODE (Main) 1 EXEC	Display: MODE TRIGGERED (1). Scope: CH1, 1 cycle of sine wave, CH2, Sync pulse, 0 to ≥2.5V
60	Gated		↑	Display: MODE GATED (2). Scope: CH1-Burst of sinewave. CH2-Burst of sync pulses.
61	Burst		↑	Display: MODE BURST (3). Scope: CH1-2 cycles of sine wave. CH2-2 sync pulses.
62			BURST ↑ ↑	Display: BURST COUNT 4. Scope: CH1-4 cycles of sine wave. CH2-4 sync pulses.

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
63	Trigger Haver		MODE (Main) ↑	Display: MODE TRIG HAVER(4). Scope: CH1-1 cycle of haversine CH2-One sync pulse.
64	Gated Haver		↑	Display: MODE GATED HAVER(5) Scope: CH1-Burst of haversine. CH2-Burst of sync pulses.
65	Burst Haver		↑	Display: MODE BURST HAVER (6). Scope: CH1-4 cycles of haversine. CH2-4sync pulses.
66			FUNC	Display: FUNC SINE (0)
67			↑	Display: FUNC TRIANGLE (1). Scope: CH1-4 cycles of havertriangle. CH2-4 sync pulses.
68			↑	Display: FUNC SQUARE (2). Scope: CH1-4 cycles of square wave. CH2-4 sync pulses.
69			↑	Display: FUNC RAMP (3). Scope: CH1-4 cycles of ramp. CH2-4 sync pulses.
70	Inverted Burst Haver		AMPL −1 EXEC	Display: AMPL −1 V P-P Scope: CH1-4 cycles of inverted ramp. CH2-4 sync pulses.
71			FUNC ↓	Display: FUNC SQUARE (2). Scope: CH1-4 cycles of inverted square. CH2-4 sync pulses.
72			↓	Display: FUNC TRIANGLE (1). Scope: CH1-4 cycles of inverted havertriangle. CH2-4 sync pulses.
73			↓	Display: FUNC SINE (0). Scope: CH1-4 cycles of inverted haversine. CH2-4 sync pulses.
74	System Reset		RESET	Display: RESET. Scope: CH1-1 kHz, 1 Vp-p sine wave. CH2-0 to ≈2.5V sync pulses.
75	Continuous Sweep, Linear.	Attach scope per figure 2-3. Scope: Trigger to internal. Horizontal to .5 ms/div. Vertical mode to chop. Sync to CH1.	MODE (Sweep) 1 EXEC	Display: SWP CONT LIN (1). Scope: CH1-Frequency sweeping from 500 Hz to 5 kHz, 2s per sweep. CH2- 0 to ≈5V, 2 sec ramp.

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
76	Trigger Sweep, Reset, Linear		↑	Display: SWP TRIG RST LIN (2). Scope: CH1-500 Hz sine wave. CH2-0 Vdc.
77			MAN TRIG	Scope: CH1-Sweeping to 5 kHz and reset back to 500 Hz. CH2-Ramp to ≈5V and reset to 0V.
78	Trigger Sweep and Hold, Linear		↑ Scope: CH1-500 Hz sine wave. CH2-0 Vdc.	Display: SWP TRIG HOLD LIN (3) Scope: CH1-500 Hz sine wave. CH2-0 Vdc.
79			MAN TRIG	Scope: CH1-Sweep to and hold at 5 kHz. CH2-Ramp to ≈5 Vdc
80			MAN TRIG	Scope: CH1-Reset to 500 Hz. Ch2-Reset to 0 Vdc.
81	Sweep Hold and Resume		TIME 10 EXEC MAN TRIG	Display SWEEP TIME 10 SEC Scope: CH1-Frequency sweep starts. CH2-Ramp to ≈5Vdc
82			HOLD	Scope: CH1-Constant frequency. CH2-Stops ramping. Display: Indicates frequency at hold.
83			RESUME	Scope: CH1-Sweep continues, stops at 5 kHz. CH2-Continues to ≈5 Vdc. Display: RESUME
84			MAN TRIG	Scope: CH1-Reset to 500 Hz. CH2-0 Vdc. Display: SWEEP TIME 10 SEC
85	Sweep Hold, Search and Resume		MAN TRIG	Scope: Sweep starts.
86			HOLD	Scope: Constant frequency.
87			← ↑ ↓ →	Scope: CH1-Frequency increasing or decreasing. CH2-Sweep output level remains constant.
88			RESUME	Scope: CH1-Sweep continues from where it was held. CH2-2 ramps to ≈5 Vdc.
89	Continuous Sweep, Logarithmic		START FREQ 100 STOP FREQ 1E5 MODE (Sweep) 4 EXEC	Display: SWP CONT LOG (4). Scope: CH1-Frequency sweeping from 100 Hz to 100 kHz logarithmically. CH2-2 ramps to ≈5 Vdc.
90	Triggered Sweep, Reset, Logarithmic		↑	Display: SWP TRIG RST LOG (5). Scope: CH1-100 Hz. CH2-0 Vdc.

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
91			MAN TRIG	Scope: CH1-Frequency sweeps from 100 Hz to 100 kHz logarithmically, then resets to 100 Hz. CH2-Ramps to ≈5 Vdc, resets to 0 Vdc.
92	Triggered Sweep and Hold, Logarithmic		↑	Display: SWP TRIG HOLD LOG (6). Scope: CH1-100 Hz. CH2-0 Vdc.
93			MAN TRIG	Scope: CH1-Frequency sweeps from 100 Hz to, and holds at, 100 kHz, logarithmically. CH2-2 ramps to ≈5 Vdc.
94			MAN TRIG	Scope: CH1-Reset to 100 Hz. CH2-Resets to 0 Vdc.
95	Sweep with Marker	Scope: Connect scope as in figure 2-5. Sync to external input. Horizontal 2 ms/div	MODE (SWEEP) 4 TIME .02 MARKER 1 EXEC	Display: MKR (1) 1 KHZ. Scope: CH1-Frequency sweeps from 100 Hz to 100 kHz. logarithmically. CH2-Marker switches from low to high when swept frequency is at 1 kHz.
96	Enter Marker Frequency		MARKER 2 MARKER FREQ 3E3 MARKER 3 MARKER FREQ 1E4 MARKER 4 MARKER FREQ 3E4	
97	Recall Marker Frequency		MARKER 1 EXEC	Display: MKR (1) 1 kHZ. Scope: Marker at 1 kHz of swept frequency.
98			↑	Display: MKR (2) 3 kHZ. Scope: Marker at 3 kHz of swept frequency.
99			↑	Display: MKR (3) 10 kHZ. Scope: Marker at 10 kHz of swept frequency.
100			↑	Display: MKR 30 kHZ. Scope: Marker at 30 kHz of swept frequency.
101	Modify Marker Frequency		MARKER ← ↑ ↓ or → FREQ	Scope: Marker on CH2 will move left or right, and display will indicate the up-dated frequency.
102	Store Stored Settings. (If Option 001 is installed, use procedure similiar to steps 102 through 110 to verify storage locations 6 thru 45.)	Connect scope as in figure 2-6. Horizontal to 1 ms/div.	RESET FUNC 1 EXEC	Scope: 1 kHz triangle.
103			STORE 1 EXEC	Display: NO. 1 LAST STORED
104			FUNC 2 AMPL 2 EXEC	Scope: 1 kHz, 2 Vp-p squarewave.

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
105			STORE 2 EXEC	Display: NO. 2 LAST STORED
106			FREQ 2E3 FUNC 0 EXEC	Scope: 2 kHz, 2 Vp-p sine wave.
107			STORE 3 EXEC	Display: NO. 3 LAST STORED
108	Recall Stored Settings.		RECALL 1 EXEC	Display: SETTING 1 RECALLED Scope: 1kHz, 1Vp-p triangle
109			↓	Display: SETTING 2 RECALLED Scope: 1kHz, 2 Vp-p square wave.
110			↓	Display: SETTING 3 RECALLED Scope: 2kHz, 2 Vp-p sine wave.
111	Output OFF/ON		RESET	Display: RESET. Scope: 1 kHz, 1 Vp-p sine wave.
112			OFF/ON 0 EXEC	Display: OUTPUT OFF, LD OUT (0) Scope: No signal, FUNCTION OUT open circuit.
113			OFF/ON 2 EXEC	Display: OUTPUT OFF, LD IN (2). Scope: No signal, FUNCTION OUT shorts to ground through a 50Ω resistor.
114			↓	Display: OUTPUT ON (1). Scope: 1 kHz, 1 Vp-p sine wave.
115	Front or Rear Output		FRONT/ REAR	Display: FRONT OUTPUT (0). Scope: (CH1) 1 kHz, 1 Vp-p sine wave. (CH2) no signal.
116			FRONT/ REAR 1 EXEC	Display: REAR OUTPUT (1). Scope: (CH1) no signal. (CH2) 1 kHz, 1 Vp-p sine wave.
117			↓	Return to front output.
118	External Trigger	Connect scope and Model 182A (TTL source) as in figure 2-7. Set Model 182A frequency to 100 Hz. Sync on CH2. Horizontal to 2 ms/div. Scope trigger to internal.	RESET	Display: RESET.
119			MODE (Main) 2 EXEC	Display: MODE GATED (2). Scope: Burst of sine wave (CH1) when square (CH2) is high.
120			SLOPE 1 EXEC	Display: TRIG SLOPE NEG (1). Scope: Burst of sine wave (CH1) when square (CH2) is low.

Table 2-3. Operation Verification (Continued)

Step	Test	Tester & Setup	Program	Desired Results
121	Amplitude Modulation	Connect scope and sine generator as shown in figure 2-8. Sync on CH2. Set Model 182A to 100 Hz, 3 Vp-p sine wave. Scope trigger internal. Horizontal to 2 ms/div.	RESET	Display: RESET.
122			FREQ 1 EXP 4 FUNC 5 EXEC	Display: FUNC AM SINE (5). Scope: Modulated sine wave (CH1), 100 Hz, 3 Vp-p sine wave (CH2).

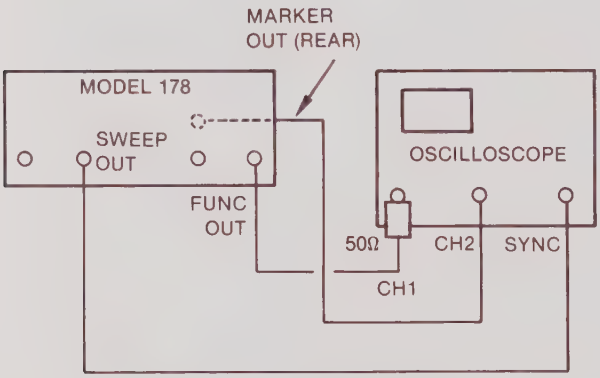


Figure 2-5. Step 95 Setup

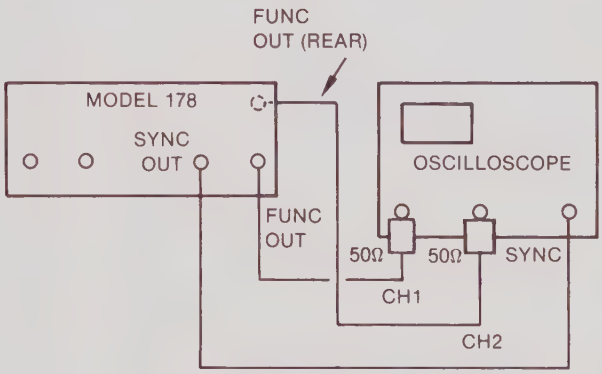


Figure 2-6. Step 102 Setup

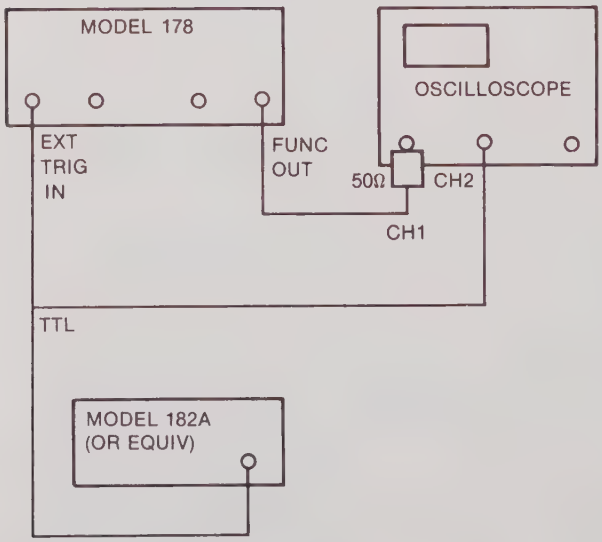


Figure 2-7. Step 118 Setup

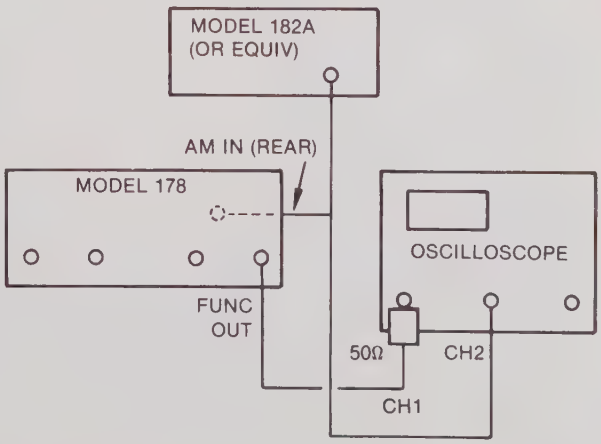
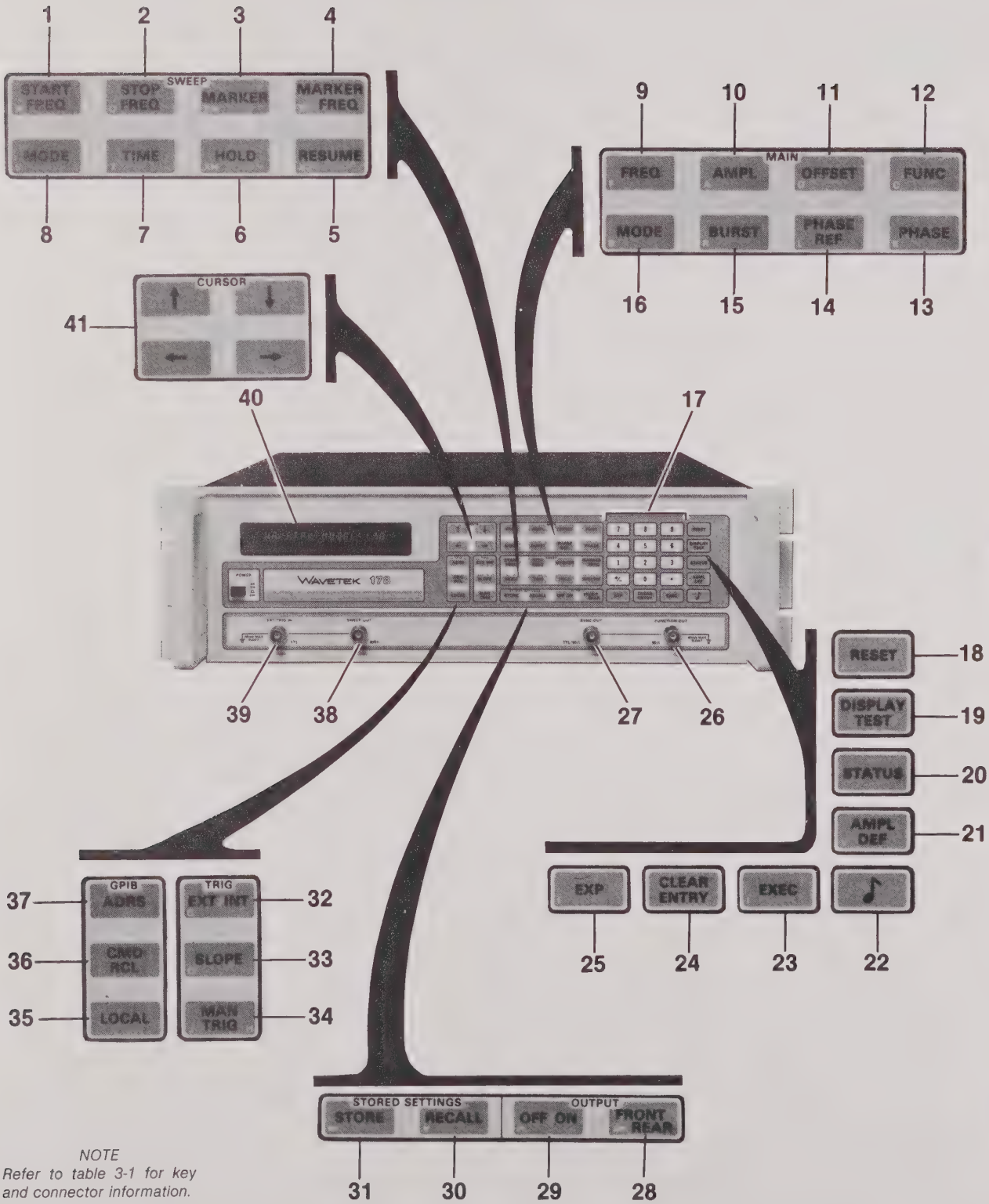


Figure 2-8. Step 121 Setup



NOTE
Refer to table 3-1 for key and connector information.

Figure 3-1. Front Panel Controls and Connectors

SECTION 3
OPERATIONS

3.1 DATA ENTRY

Using the Model 178 is quite straight forward and is easily understood by trial and error method while the microprocessor "converses" with you during operating, informing you what was programmed, what is possible to program and when an error is made. Perform the procedures of table 2-3 to familiarize yourself with Model 178 operation. Keyboards are shown in figure 3-1 and cross referenced to table 3-1, which in turn references the applicable text. Readout that occurs when the keys are pressed are listed in Appendix C. Readout is literal and in two slightly different modes. For example, for frequency, amplitude and offset, when FREQ, AMPL or OFFSET keys are pressed, as for an inquiry as to status, the words MICROHERTZ, MILLIVOLTS, etc., are used; when the operator starts keying in the parameter argument, no unit of measure is displayed. Coded parameters, such as function, mode and output show their programmed argument in parentheses.

An audible tone indicates that a key is pressed. Pressing ♪ will prevent or restore the key tone. If there is no tone when keys are pressed, pressing ♪ restores the tone and vice versa.

Information exclusive to the GPIB is given in paragraph 3.16.

Additional reference information appears in the appendixes:

Appendix A - ASCII and IEEE (GPIB) Code Chart
Appendix B - Programming Command Summary
Appendix C - Displays
Appendix D - Output and Timing for Basic Modes and Functions.
Appendix E - Mode Combinations and Output

Table 3-1 Function Cross Reference

Location in Figure 3-1	ASCII Character	Function	Action (A) or Parameter (P)	Appendix C and Paragraph
1	N	Sweep Start Frequency	P	3.9.1
2	O	Sweep Stop Frequency	P	3.9.1
3	XN	Marker Selection	P	3.9.6
4	XO	Marker Frequency	P	3.9.6
5	XJ	Resume Sweep	A	3.9.5
6	XH	Sweep Hold	A	3.9.5
7	T	Sweep Time	P	3.9.2
8	S	Sweep Mode	P	3.9.4
9	F	Frequency	P	3.8.1
10	A	Amplitude	P	3.8.2
11	D	DC Offset	P	3.8.3
12	C	Function (Waveform)	P	3.8.4
13	K	Phase	P	3.8.6
14	L	Set Phase Zero Reference	A	3.8.6
15	R	Burst Count	P	3.8.5
16	B	Main Generator Mode	P	3.8.5
17	0 thru 9	Number Characters	P	3.3
18	Z	Reset	A	3.13
19		Display Test	A	3.14
20		Status	A	3.15

Table 3-1 Function Cross Reference (Continued)

Location in Figure 3-1	ASCII Character	Function	Action (A) or Parameter (P)	Appendix C and Paragraph
21	V	Amplitude Definition	P	3.8.2
22		♪(Tone On/Off)	A	3.1
23	I	Program Execution	A	3.5
24		Clear Entry	A	3.12
25	E	Exponent	P	3.3.3
26		Function Output		3.11.1, App E
27		Sync Output		2.2, 3.11.3
28	XP	Output Front/Rear	P	3.11.1
29	P	Output Off/On	P	3.11.2
30	Y	Recall Stored Setting	P	3.10
31	M	Store Setting	P	3.10
32	G	Trigger, Int/Ext	P	3.7
33	Q	Triggering Slope	P	3.7
34	J	Manual Trigger Pressed	A	3.7
34	H	Manual Trigger Released	A	3.7
35		Local Control Enable	A	3.16
36		Command Recall	A	
37		GPIB Address	A	2.2.4, 3.16.2.1
38		Sweep Generator Output		3.9.4, App E
39		External Trigger Input		3.9.4
	U	Recall Previous Program	A	3.10.2
	W	Recall Next Program	A	3.10.3
	XG	GET Mode	P	3.16.7
	XQ	SRQ Enable	P	3.16.5
	XT	Talk Message	P	3.16.4
	XV	Terminator Select	P	3.16.6
40		Readout		3.16.9, App C
41		Cursor	A	3.6

3.2 POWER

Power is turned on and off with a front panel push-button. When the power is turned on, the entire display lights up for a display element test. Then, the generator automatically performs a self test routine. "SELF TEST" is displayed at this time. When testing is completed, "WAVETEK 178" is displayed. At least two seconds must elapse between power OFF and power ON for proper reinitialization of logic. When the power comes on, the output is automatically enabled.

3.3 BASIC COMMAND STRUCTURE

The Model 178 is programmed by sending ASCII coded characters (ref: table 3-1 and Appendix A) to the microprocessor via one of the two possible input ports (keyboard or GPIB) shown in figure 3-2. If input characters are present on more than one input port, they are read first from the GPIB and then from the keyboard. Thus, if the GPIB port is continuously supplied with characters, then no characters will ever be read from the keyboard.

3.3.1 Characters

Characters used to program the 178 are divided into classes:

1. **Alphabetic Characters**—The characters A through Z (except E) select actions or commands. The X character used in front of another alphabetic character selects an alternate set of actions or commands. The X must directly precede the alphabetic character without intervening characters of any kind. For example, P selects the output and off/on and XP selects front/rear function output, but X ∧ P (where ∧ is a space character) selects output off/on, not front/rear output because a space character,

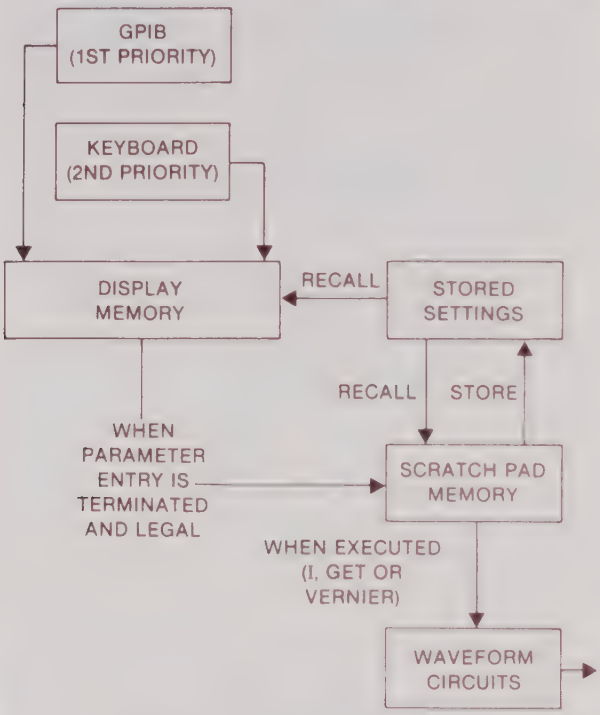


Figure 3-2. Memory Structure

not X, was placed immediately before the P. Alphabetic characters are generated from the keyboard by pressing the labeled action and parameter keys. The characters generated by such keys are printed in a corner of the key.

2. **Numeric Characters**—The characters 0 through 9, E, −, and decimal point (.).

3. **Special Character**—Quote (').

4. **Terminator Character**—Initially the ASCII new line character (NL). This can be changed by programming.

5. **Nonprogramming Characters**—Any character not in one of the previously described classes. They have no effect on programming and may be interspersed freely among programming characters, except after X (refer to item 1).

3.3.2 Action Vs Parameter

The alphabetic characters are used to select either actions or parameters (ref: table 3-1). An action is a sequence of events which happens when the letter that selects it is programmed or the key that selects it is pressed. There is no need for a numerical suffix. A programming parameter has one or two letters (and most have keys) plus a numeric value which controls some aspect of the instrument's operation.

To program an action, simply program the proper alphabetic character from either the front panel or GPIB port. The action will then take place, but only if the instrument is in the *enable* state at the moment when that character is read by the microprocessor (ref: REN, paragraph 3.16.1).

To examine the current value of a parameter, simply program the proper alphabetic character from either the front panel or GPIB port. The current value is then displayed on the front panel. Display occurs whether or not the instrument is enabled. If the character programmed does not correspond to a legal parameter in the instrument, nothing happens.

3.3.3 Programming Parameter Values

The numeric characters (0 through 9, E, −,) are used to program new parameter values. To change a parameter value, first program the alphabetic character which selects the desired parameter (F = frequency, etc.). Next, program the new value using numeric characters. Any sequence of characters which gives the new value is acceptable. For example, all of the sequences in table 3-2 cause the value 100 to be programmed.

Table 3-2. Examples of Value Programming

ASCII	Keyboard	Standard Notation
100	100	100
0100	0100	100 (leading zeros are ignored)
1E2	1 EXP 2	1×10^2
.01E4	.01 EXP 4	$.01 \times 10^4$
.01E304	.01 EXP 304	$.01 \times 10^4$ (last two exponent digits only are used)
1000E-1	1000 EXP ±1	1000×10^{-1}
1E-2-	1 EXP ±2 ±	1×10^2 (two minus signs cancel)
1E.2	1 EXP .2	1×10^2 (decimal points in exponent are ignored).

The numbers to the left of the E are the mantissa; the digits to the right (only two are allowed) are the exponent. The result value is the mantissa times 10 to the exponent power: for example 9.99 E2 = 9.99×10^2 = 999.

Only one decimal point and one E (keyboard EXP) are allowed per number; additional ones are ignored. The sign toggle character may appear any number of times. It causes the sign of the mantissa (if E has not been programmed) or the exponent (if E has been programmed) to be reversed (if negative, then positive, and vice versa) each time it appears. Any number of nonprogramming characters may be interspersed with the numeric characters, as they have no effect. If an undesired value is entered, the CLEAR ENTRY key can be used to erase it.

Several parameters required codes for specific selections; for example, function codes 0 through 3 select sine wave. triangle wave. square wave and ramp waveform. Refer to Appendix B for codes.

Table 3-3. Round Offs

Parameter	Round Offs
Frequency	Up to 8 Digits, 1 μHz minimum.
Amplitude	To Nearest 20 mV, 10.02 to 20.00V To Nearest 10 mV, 1.01 to 10.00V To Nearest 1 mV, 99 to 1000 mV To Nearest 100 μV, 9.9 to 100.0 mV To Nearest 10 μV, 1.00 to 10.00 mV
Offset	Up to 3 Digits: To Nearest 10 mV, 5.01 to 10.00V To Nearest 5 mV, 1.005 to 5.00V To Nearest 1 mV, 100.5 to 10.00 mV To Nearest 100 μV, 10.05 to 100.0 mV To Nearest 10 μV, 1.00 to 10.00 mV
Phase	Up to 5 Digits: ±360.00° ±.01°
Time (Sweep)	Up to 4 Digits or 10 μs To Nearest .01s
Time (Sweep Off)	Up to 8 Digits: 10 μs to 600.00s to nearest 10 μs
All Other Parameters	To Nearest Integer

Since the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic, special or terminator character. When this is done, the new value is rounded off (ref: table 3-3) and tested to see if it is a legal value for the setting being changed (ref: paragraph 3.4). If it is legal, the new value is entered into the instrument's scratch pad memory; however, it is not yet sent to the waveform circuits. That is usually done by programming the I action (EXEC key on the front panel). Other methods of execution are GET and cursor, which are described later. An asterisk (*) on the display indicates that the new parameter value programmed has not been executed and resides in scratch pad memory only (ref: figure 3-2). All parameter values may be erased before execution by using the CLEAR ENTRY key, the value stored in scratch pad is erased and the original value is displayed.

3.4 ERRORS

When an illegal value is programmed or interdependent parameter errors are detected, an error signal is indicated on the front panel or GPIB. Keyboard errors only are indicated on the front panel display and by a double "beep" of the key tone. For errors made via the GPIB (but not the keyboard), a service request (SRQ) is made, providing the service request function has been enabled (ref: paragraph 3.16.5). The controller can then serial poll its instruments to verify that the 178 sent the SRQ and can then inquire as to the nature of the error. The method of reporting errors on the GPIB is given in paragraph 3.16.4.

3.4.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the parameter being programmed. For example, programming an amplitude of 500 volts will cause a parameter error when the next alpha character is programmed. At this time, the 178 disregards the new values and retains the previously programmed values in scratch pad memory (see figure 3-2).

3.4.2 Class 2 Errors

Class 2 errors are interparameter inconsistencies, such as frequency greater than specified for a particular function. Tests are made every time an execute (I) is given, a setup is stored (M) or a cursor key is pressed. Resulting errors are displayed, and transfers of values are made to waveform circuits or storage regardless of the error indicated. Notice that

upon receiving a Group Execute Trigger (refer to paragraph 3.16.7), the 178 programming is executed without error checking.

3.4.3 Class 3 Error

Class 3 error occurs if an empty stored setting is retreived. The error is displayed and the state of the 178 remains unchanged from the previously executed program.

3.5 EXECUTING THE PROGRAM

A program or setting can be executed, i.e., transferred to the waveform circuits, by the execute commands, GET (Group Execute Trigger) command, and the action keys: CURSOR ↑ and CURSOR ↓.

GPIB I and the front panel EXEC key are execute commands that cause parameter value and inter-parameter tests to be made and transfers the programmed values to the waveform generation circuits.

GET is a GPIB only command (no front panel key) that causes the 178 to execute and trigger, but without time consuming microprocessor error checking (ref: paragraph 3.16.7).

CURSOR ↑ and CURSOR ↓ are exclusively front panel functions which perform an execute with error checks after each digit increment or decrement.

GPIB **Z** and the front panel RESET are commands which reset the 178 to the original power up conditions (as described in table 2-3, step 3) and perform an automatic execute.

An asterisk (*) on the display indicates that the new parameter value programmed has not been executed and resides in scratch pad memory only (ref: figure 3-2).

3.6 CURSOR

The four cursor keys can modify a parameter value or code.

NOTE

The modified value is automatically executed.

The ← and → cursor keys move the cursor left and right; cursor position is indicated by a flashing digit on the display. The ↑ and ↓ cursor keys increment and decrement, respectively, the flashing digit. Holding a cursor key down causes a continued change at a constant rate.

The ↑ and ↓ keys can also increment and decrement parameter codes, such as function and mode codes. Cursor positioning (← →) is not necessary for codes and codes do not flash to indicate cursor position.

When storing a program, press STORE key and then ↑. The program will be stored in the next memory location in numerical sequence. Keys ↑ and ↓ can also be used to recall stored settings in numerical sequence.

During command recall, cursor ← and → keys shift the display four characters to the left or right, respectively.

Cursors ↑ and ↓ can also be used to recall marker frequency and status

3.7 TRIGGER MODE AND SLOPE

Triggered and gated modes of the main generator are initiated either by external or internal triggers. External triggers are: external TTL level signal at front or rear panel BNCs, manual trigger at MAN TRIG key on the front panel or GPIB **J** and **H** commands. Internal trigger is the sweep generator; that is, each sweep generator cycle triggers or gates the main generator.

The sweep generator is triggered by the above named external triggers only.

NOTE

*"External/Internal" trigger mode (**G0** or **1**) has no effect on sweep generator triggering. If the sweep generator is in a trigger-mode, external triggers (TTL level signals at front or rear panel BNCs, manual trigger at MAN TRIG key on the front panel or GPIB **J** and **H** programming codes) will initiate sweep generator output.*

Both the main generator and sweep generator can be triggered by the same source, one may be triggered and the other not, or the external trigger may trigger the sweep generator which in turn triggers the main generator—all depends upon the generator modes (ref: table 3-4).

G followed by its code selects either internal or external trigger (affects main generator only):

G0 Selects external trigger.

Table 3-4. Mode Matrix

	MAIN GENERATOR			SWEEP GENERATOR			
					Linear Sweep (Logarithmic Sweep)		
			Trig Mode	Sweep Off S0	Continuous Sweep S1 (S4)	Trigger Sweep S2 (S5)	Trigger Sweep/ Trigger Reset S3 (S6)
Standard Waveforms (Haverwave Waveforms)	Continuous	B0	*	B0,S0	B0,S1	B0,S2	B0,S3
	Triggered	B1 (B4)	Ext G0	B1,S0,G0	B1,S1,G0	B1,S2,G0	B1,S3,G0
			Int G1	B1,S0,G1	B1,S1,G1	B1,S2,G1	B1,S3,G1
	Gated	B2 (B5)	Ext G0	B2,S0,G0	B2,S1,G0	B2,S2,G0	B2,S3,G0
			Int G1	B2,S0,G1	B2,Si,G1	B2,S2,G1	B2,S3,G1
	Burst	B3 (B6)	Ext G0	B3,S0,G0	B3,S1,G0	B3,S2,G0	B3,S3,G0
			Int G1	B3,S0,G1	B3,S1,G1	B3,S2,G1	B3,S3,G1

Log Sweep Modes S4, S5 and S6

Haverwave modes B4, B5 and B6.

Refer to these codes in Appendix E for output explanation regardless of waveform (standard or haverwave) and sweep (linear or log).

* Trigger mode is applicable to main generator only. Trigger mode does not affect main generator continuous modes.

G1 Selects internal trigger.

J (pressing MAN TRIG) - Start trigger for the main and sweep generator. In main generator gated mode, the main generator is gated on.

H (releasing MAN TRIG) - In main generator gated mode, terminates the output of the main generator (the last cycle started is always completed).

Q followed by its code selects triggering either on the rising edge of the trigger signal or the falling edge:

Q0 Selects triggering on the rising edge (⨍) of the trigger signal. The main generator gates on at the high level.

Q1 Selects triggering on the falling edge (⨍) of the trigger signal. The main generator gates on at the low level.

3.8 MAIN GENERATOR

The following sections describe the keys and codes related to main generator operation. This block of keys are labeled MAIN on the front panel.

3.8.1 Frequency

Selecting **F** following a value (up to 8 digits) programs the main generator frequency. The frequency is programmable in hertz. See table 3-2 for value programming. At any time the frequency may be modified by the cursor (ref: paragraph 3.6). Upper frequency is limited by the operating mode and function, as shown in table 3-5.

Table 3-5. Mode/Function/Frequency

Mode	Function	Frequency
Cont	∿ , ⊓ , AM	to 50 MHz
	∿	to 500 kHz
	◿ ◺	to 20 kHz
Trigger, Gate, and Burst	∿ , ⊓ , ∿ , AM	to 200 kHz
	◿ ◺	to 20 kHz

3.8.2 Amplitude

V followed by its code selects the unit of measure for amplitude programming into a 50Ω load. (DC offset is always Vpeak.):

V0 Selects volts peak-to-peak into 50Ω.

V1 Selects volts rms into 50Ω.

V2 Selects dBm into 50Ω.

An **A** followed by a value (up to 3 digits) programs the amplitude at the function output. Amplitude may be programmed in volts peak-to-peak from 1 mV to 20 Vp-p specified into a 50Ω load. See table 3-2 for value programming, table 3-3 for round off and paragraph 3.11 for function output and load operation.

Amplitude values may be modified by the cursor (ref: paragraph 3.6).

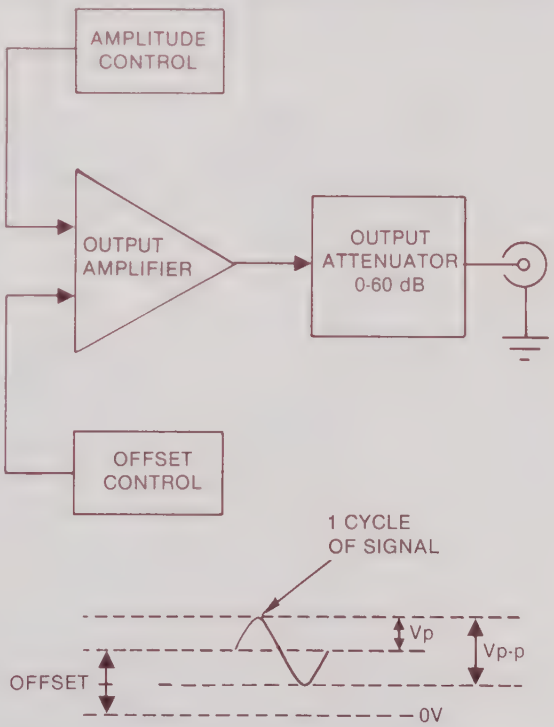


Figure 3-3. Amplitude and Offset Schematic

The amplitude and offset are not completely independent of one another, because they share a common output amplifier and attenuator (see figure 3-3). In cer-

tain cases it may be necessary to decrease the number of digits of resolution of amplitude or offset in order to prevent clipping in the output amplifier or to make the programmed value of offset (or amplitude) appear at the output despite an unfavorable attenuator setting necessitated by a larger value of amplitude (or offset).

The sum of amplitude and offset control the output amplifier and attenuator. The output amplifier is limited to ±10.00 volts peak and a 3 digit input (X.X X). The attenuator can operate at only $\times 10^{0}$, $\times 10^{-1}$, $\times 10^{-2}$, or $\times 10^{-3}$. Figure 3-4 is a guide to expected resolution.

3.8.3 Offset

D followed by a value (up to 3 digits) offsets the function output from 0 to +10V specified into a 50Ω load. Offset is programmed in volts dc. See table 3-2 for value programming, table 3-3 for round off and paragraph 3.11 for function output and load operation. Offset value may be modified by the cursor (ref: paragraph 3.6).

NOTE

When offset is used, 3 digit resolution of offset or amplitude may be reduced in some cases (ref: paragraph 3.8.2).

3.8.4 Function

C followed by a single digit parameter value selects function at the FUNCTION OUT BNC. Six function codes are used.

C0 Selects sine wave. Frequency maximum is 50 MHz in continuous mode and 200 kHz in trigger, gated or burst modes.

C1 Selects triangle wave. Frequency maximum is 500 kHz in continuous mode and 200 kHz in trigger, gated or burst modes.

C2 Selects square wave. Frequency maximum is 50 MHz in continuous mode and 200 kHz in trigger, gate or burst mode.

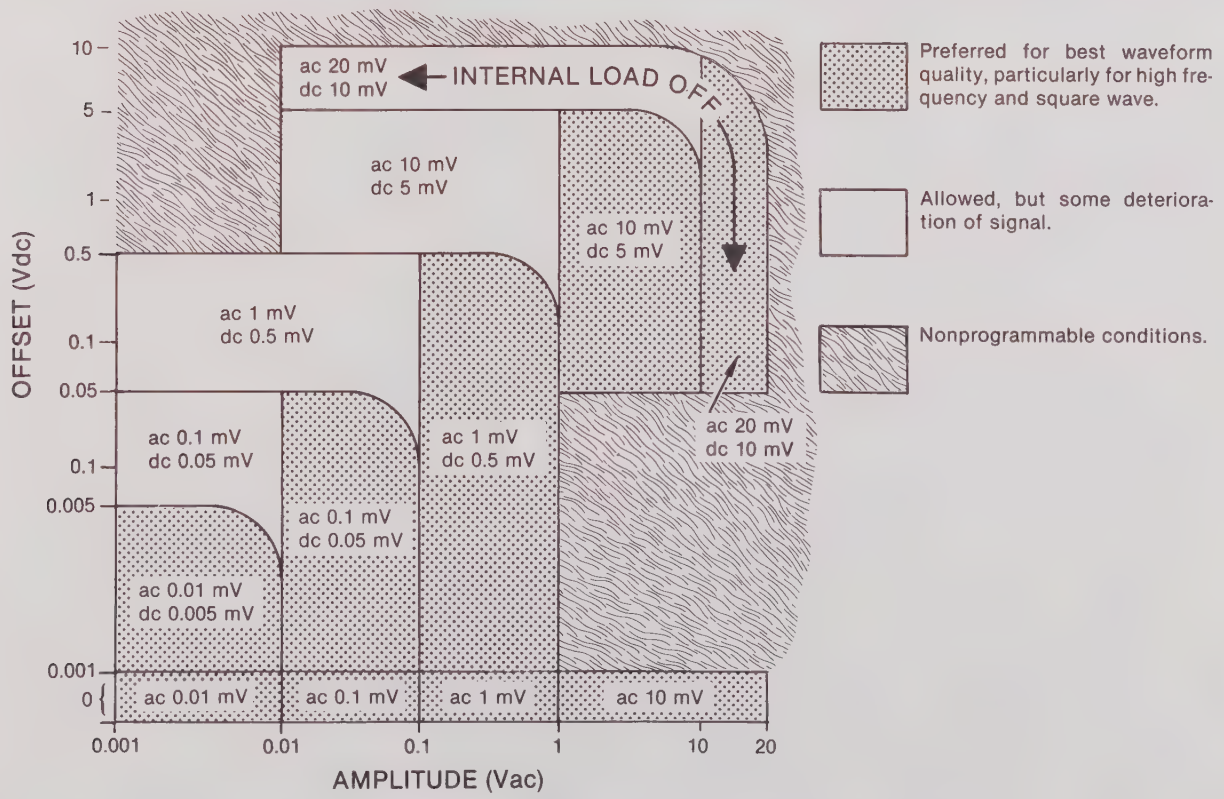


Figure 3-4. Resolution for Combinations of Amplitude and Offset

C3 Selects ramp. Frequency maximum is 20 kHz in continuous, trigger, gated burst modes.

C4 Selects dc output voltage. The dc level is set by programming offset as described in paragraph 3.8.3.

C5 Selects amplitude modulation. When AM is selected the main out level is reduced to half the programmed amplitude. An ac voltage (±2.5 Vp, typical, for 100% modulation; dc to 10 MHz minimum rate) at the AM IN BNC modulates the function output. When modulation levels vary between −2.5V and −7.5V the output level is inverted as shown in figure 3-5. Figure 3-6 show AM timing relationship.

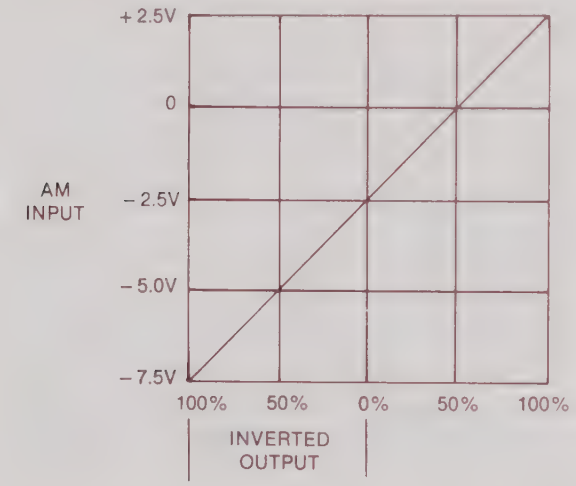


Figure 3-5. AM Input Vs Envelope Output

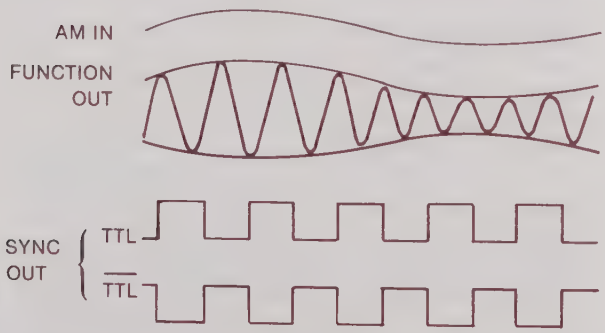


Figure 3-6. AM Timing Relationships.

3.8.5 Modes

B followed by its code (0 through 6) selects the operating mode. The selected mode is indicated on the front panel readout when the MODE key is pressed. In addition to the main generator mode selection, output is affected by other variables (ref: table 3-4 and Appendix E). Many of the modes depend on a trigger. Refer to paragraph 3.7 for trigger mode and format selection.

B0 Selects continuous operation of the main generator.

B1 Selects triggered mode. The main generator is triggered by external signal, internal sweep signal, manual trigger of GPIB commands. When triggered, one cycle is generated.

B2 Selects gated mode. The onset of the trigger, regardless of its source (ref: mode **B1**), enables the main generator for the duration of the trigger signal plus the time required for the completion of the last cycle started.

B3 Selects burst mode. Burst is the output of a preprogrammed number of cycles each time the generator is triggered at a preselected rate.
R followed by its value (1 to 65,536) denotes the number of cycles in the burst each time it is triggered.

B4 Selects triggered haverwave. For ramp and square waveforms, triggered haverwave is identical to mode **B1**, triggered waveforms. For sine and triangle, triggered haverwave is one cycle of the waveform starting and ending at phase angle −90°. Square wave starts and ends at its negative peak. If waveform amplitude is programmed negative, the waveform starts and ends at +90° phase angle. Square wave starts and ends at its positive peak.

B5 Selects gated haverwave. For ramp and square waveforms, gated haverwave is identical to mode **B2**, gated waveforms. For sine and triangle waveforms, gated haverwave is one or more cycles of the selected waveforms starting at phase angle −90°, if any. If waveform amplitude is programmed negative, the waveform starts at +90° phase angle. The onset of the trigger, regardless of its source (ref: mode **B1**), enables the main generator for the

duration of the trigger signal plus the time required for the completion of the last cycle started.

B6 Selects burst haverwave. For ramp and square waveforms, burst haverwave is identical to mode **B3**, burst mode. For sine and triangle, burst is the output of a preprogrammed number of cycles of selected haverwave starting at phase angle −90°. If waveform amplitude is programmed negative, the waveform starts at +90° phase angle.

R followed by its value (1 to 65,536) denotes the number of cycles in the burst.

3.8.6 Phase

To shift output signal phase relative to some external signal, the basic 10 MHz reference must be locked to the reference clock of the external instrument; an external reference input can be a sine wave or pulse of a 500 mV to 10 Vp-p amplitude at 1, 2, 3, . . . or 10 MHz ±5 ppm. A message REFERENCE NOT LOCKED is displayed if the 178 internal reference and the external reference source are not synchronized or if the external reference has high jitter.

The frequencies of the two signals to be phase locked should be adjusted to be identical or integer multiples. The phase angle of these two signals is not defined, but by programming **L**(PHASE REF) that phase angle becomes the reference phase "zero" for subsequent phase changes.

K followed by a value selects the phase shift (relative to phase "zero") measured in degrees. Phase value is programmable from ±1000 revolutions (±360,000°) with 0.01° resolution steps to 500 kHz and 0.1° above 500 kHz. When executed, the phase shifts to the programmed angle relative to Phase Reference. Phase Reference may be redefined at any time by programming **L** (PHASE REF). Phase relationships relative to the reference generator are shown in figure 3-7.

NOTE

When function is square wave, there may be a ±3.6° phase offset error after you have phase shited the first time. This error is eliminated by programming **L** *and noting the new phase reference angle from which to shift. Subsequent shifts will be to specified accuracy.*

An input to ϕMOD IN BNC phase modulates the 178. A 5 Vp signal deviates the function output approximately 360° when output frequency is >500 kHz. For frequencies ≤500 kHz, phase modulation is reduced by 100 times. Phase modulation is relative to the reference source and at a deviation rate determined by ϕMod frequency (dc to 10 kHz minimum).

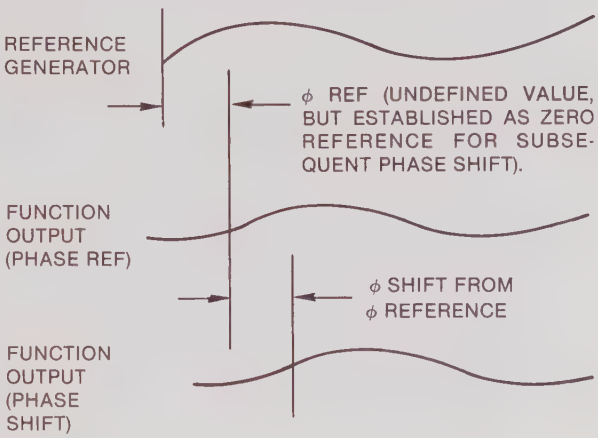

REFERENCE GENERATOR
ϕ REF (UNDEFINED VALUE, BUT ESTABLISHED AS ZERO REFERENCE FOR SUBSEQUENT PHASE SHIFT).
FUNCTION OUTPUT (PHASE REF)
ϕ SHIFT FROM ϕ REFERENCE
FUNCTION OUTPUT (PHASE SHIFT)

Figure 3-7. Phase Shift

Rear Panel REF OUT BNC is a source of 10 MHz, 2 Vp-p sine wave locked to the reference clock. Source impedance is 50Ω.

3.9 SWEEP GENERATOR

An internal generator sweeps the main generator either linearly or logarithmically from the start frequency to the stop frequency. Two overlapping sweep ranges are used: the low range 1 μHz to 500 kHz and the high range 5 kHz to 50 MHz. A class 2 error occurs when start and stop frequencies are not in the same range.

In addition to sweeping the main generator, when trigger mode is "internal" and the main generator is in a trigger or gate mode, the sweep generator triggers the main generator.

The following sections discuss sweep generator controls and operation.

3.9.1 Start and Stop Frequency

The main generator sweeps from the start frequency to the stop frequency. For sweep up (increasing frequency) the start frequency is lower than the stop frequency. For sweep down (decreasing frequency), the start frequency is higher than the stop frequency.

N followed by its value (up to 8 digits or 1 μHz) programs the start frequency. The start frequency is programmed in hertz. (See table 3-2 for value programming.)

O followed by its value (up to 8 digits or 1μHz) programs the stop frequency. The stop frequency is programmed in hertz.

3.9.2 Sweep Time

T followed by a value selects the time required to sweep between the start and stop frequencies. The value is programmed in seconds. (See table 3-2 for value programming.) Time can be programmed from 10 ms to 600.00s with 10 ms resolution in all sweep modes except "sweep off," which can be programmed from 10 μs to 600.00s with 10 μs resolution.

When sweeping, altering sweep time, sweep frequency or stop frequency causes the generator to reset to the start frequency.

3.9.3 Sweep Width

Sweep width is the difference between the start and stop frequencies. Maximum sweep width is limited by the sweep range, either 5 μHz to 500 kHz or 5 kHz to 50 MHz.

Minimum sweep is dependent on the sweep range and time. Any start and stop frequencies may be used provided a minimum separation is maintained:

Low band: 20 mHz per 1s of sweep time.
High band: 2 Hz per 1s of sweep time.

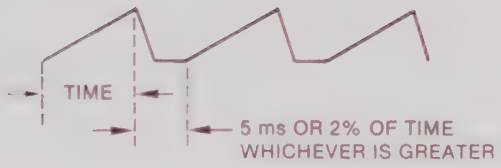
Minimum width in logarithmic sweep mode is limited to the above restrictions and a start/stop frequency ratio of 2.

3.9.4 Sweep Mode

S followed by its single numeric value selects the sweep operating mode. The selected mode is indicated on the front panel readout when the MODE key is pressed. In addition to the sweep generator mode selection, output mode is affected by other variables (ref: table 3-4 and Appendix E). Many of the modes depend on a trigger. Refer to paragraph 3.7 for trigger mode and format selection.

S0 Selects sweep off mode.

S1 Selects continuous ramp. Normally used with continuous main generator mode to give continuous linear sweep. SWEEP OUT is a continuous 0 to approximately +5V ramp.



S2 Selects triggered linear ramp. For each trigger, the main generator, in continuous mode, sweeps once and returns to the start frequency. SWEEP OUT is one 0 to approximately +5V ramp starting with the trigger.

S3 Selects triggered linear ramp and triggered reset. Upon receiving a trigger, the main generator, in continuous mode, will sweep from the start frequency to the stop frequency and hold at the stop frequency. Upon receipt of a second trigger the main generator returns to the start frequency. SWEEP OUT is a 0 to approximately +5V ramp starting with the first trigger and holding at approximately +5V until the second trigger occurs.

S4 Selects continuous logarithmic ramp. Normally used with continuous main generator mode to give continuous logarithmic sweep. SWEEP OUT is a continuously recurring 0 to approximately +5V linear ramp.

S5 Selects triggered logarithimic ramp. Logarithmic version of mode **S2**.

S6 Selects triggered logarithmic ramp and triggered reset. Logarithmic version of mode **S3**.

3.9.5 Hold and Resume

XH (Hold) will stop the sweep and hold the main generator frequency until **XJ** (Resume) resumes the sweep. When held, the precise frequency is displayed as HOLD AT XX.XXXXXX Hz. When resumed, SWEEP RESUME is displayed.

While the sweep is being held, the FUNCTION OUT frequency can be modified by the cursor keys. When RESUME is pressed, the frequency returns to the "hold" frequency and then sweep continues. However, the ramp voltage at SWP OUT is not modified by cursor action even if the frequency during

hold is. To return the output to the start frequency rather than completing the sweep from the hold frequency, manual trigger or an external trigger is used. If the sweep generator is in triggered sweep/reset mode, two triggers will be necessary to restart the output at the start frequency.

Ramp voltage may drift during hold because of leakage current in the charging circuit; even so, the frequency remains constant. For most applications, this drift is negligible for holds less than 600 seconds.

3.9.6 Marker, Marker frequency and Marker Output

The frequencies of 10 markers can be preset but only one marker can be selected at a time. The marker output is a TTL-level low-to-high transition to indicate that the frequency has swept through the programmed marker frequency, as shown in figure 3-8. The marker output remains low at frequencies less than the marker frequency and at frequencies greater than the marker frequency the marker output remains high regardless of sweep direction.

At power on, all ten markers are preset to 1 kHz. If new marker frequencies are entered into each marker location, a reset, either from the keyboard or GPIB resets only marker #1 to 1 kHz. All other marker frequencies are unaltered. Marker frequencies can also be stored for convenience (ref: paragraph 3.10.1).

XN followed by a value (1 through 10) selects the marker number. Only the selected marker's frequency is indicated by the marker output. After a marker has been selected, the marker's frequency may be altered by programming **XO**, and the frequency (up to 8 digits) in hertz. The value replaces the former value upon the programming of the next alpha character.

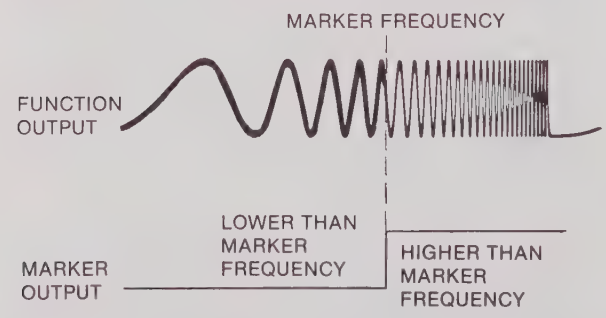


Figure 3-8. Marker Output and Sweep Frequency

3.10 STORED SETTINGS

Up to 5 different sets of front panel settings can be stored in and recalled from Random Access Memory (RAM). Option 001 provides nonvoltile memory for 40 additional stored settings. Option memory is battery backed up (internally recharged) for 60 day (minimum) retention of settings. Memory is expandable to 240 stored settings.

3.10.1 Storing Program Sets

Program sets may be stored by keyboard or GPIB command. To store the program set that is in scratch pad memory (ref: figure 3-2), enter **M** followed by the storage location (1 through 5, or if option 001 is installed, 1 through 45). The next alpha programmed is the terminator, which allows the storage to occur. If a program was previously stored in that location, it will be erased and replaced by the new set. When a program is stored, the settings are tested for class one errors in the same manner as with an execute command (ref: paragraph 3.5). The program is always stored, whether or not errors were detected. Programs can be stored without interrupting the output of the 178 if a terminator other than EXEC (I) is used: this is possible because it is the scratch pad memory that is stored rather than the actual settings of the waveform circuits (ref: figure 3-2). Notice that during 178 operation, scratch pad memory can be changed and stored without affecting 178 output.

3.10.2 Recalling Stored Programs

The information stored in a program may be recovered either from the front panel or by a command over the GPIB. To recall, program a **Y** followed by the number of desired program. When the next alpha entry is made, the settings stored in the selected program are transferred to display memory and the scratch pad memory (ref: figure 3-2). Then data is available to be sent to the waveform circuitry of the instrument, or, if desired, it may be examined and altered by use of the front panel keys.

The identifying numbers of programs in RAM range from 1 through 5 (1 through 245 for full memory options). If the number of a program which does not exist or an illegal identifying number is programmed, an error will result.

Pressing the cursor ↑ key or programming **W** causes the program next in sequence after the last program accessed to be recalled. This provides an automatic way to recall a sequence of programs. However, the

programs need not be numbered consecutively. If there is no program following the last program accessed, an error occurs.

Pressing the cursor ↓ key or programming **U** is similar to the cursor ↑ or **W** action previously described, except that programs are recalled in descending numeric order.

3.10.3 High Speed Recall of Stored Programs

The Group Execute Trigger (GET) allows a rapid GPIB recall of stored programs. In the GET mode of operation, the program is recalled and executed, and the waveform circuits are triggered, all within 2.5 ms of receiving the GET command. There are three possible modes of GET operation (ref: paragraph 3.16.7). There is no error checking.

3.10.4 Deleting Programs

To delete a program, program the letter **M** followed by a *minus* sign and a number of the program to be removed. When the number is terminated (by the next alpha character), the program is removed from storage; there is no other effect.

3.11 OUTPUTS

3.11.1 Front/Rear Function Output

One function output BNC is located on the front panel and one on the rear panel. At power up and reset the signal is from the front panel BNC only, the rear panel output is safely turned off for ATE applications. After power is on, programming selects front or rear output.

XP followed by a numerical code selects the front or rear panel BNC:

XP0 Selects front panel output and disconnects the signal from the rear panel.

XP1 Selects rear panel output and disconnects the signal from the front panel.

3.11.2 Output On/Off

P followed by a code switches the output on or off.

P0 Internally disconnects the signal from the selected function output BNC (as described in paragraph 3.11.1) making the signal unavailable at the connector. In **P0**, the function output presents a high source impedance at the BNC.

P1 Internally connects the signal to the selected function output BNC.

P2 Internally disconnects the signal from the selected function output making the signal unavailable. The function output source impedance is 50Ω.

3.11.3 Sync Outputs

Sync outputs of TTL and $\overline{\text{TTL}}$ square wave are provided, respectively, at the BNC's on the front and rear panels. The sync signal is 0V to approximately 3V (TTL) from a 50Ω source. Sync outputs are in phase with the main generator square wave output only. Other timing relationships are shown in Appendix D.

3.12 CLEAR ENTRY

The CLEAR ENTRY key erases a parameter value which is being entered. The key removes the numeric digits entered after the last parameter letter entry. (Clearable entries are always prefixed by an asterisk on the display.) The display is replaced by the previous value (scratch-pad value) of the parameter being programmed.

3.13 RESET

The RESET key returns the 178 waveform parameters to their power-on condition. The readout becomes "RESET". Significant parameters values and conditions are given in table 2-3, step 3. In addition, the reset command resets marker #1 to 1 kHz, but markers 2 through 10 remain unaltered.

3.14 DISPLAY TEST

The DISPLAY TEST Key lights all 20 sets of character segments and semicolon as shown in figure 2-4.

3.15 STATUS

Pressing STATUS automatically displays the current waveform generator status one parameter and value at a time (ref: Appendix C). When STATUS is pressed a second time the cycling immediately stops. The parameters can then be manually searched by using the CURSOR (↓ or ↑) keys (ref: table 2-3, steps 2 through 7).

3.16 GPIB

Almost all of the information in Section 3 is applicable to the General Purpose Interface Bus (GPIB) program-

ming of the 178, but the information in this paragraph is *exclusive* to the GPIB.

The GPIB interface is an implementation of IEEE Standard 488-1978. It supports the following interface functions: Source Handshake (SH1), Acceptor Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

3.16.1 Bus Lines Defined

The GPIB consists of 16 signal lines:

DIO1 - DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

1. **DIO1 - DIO8**—These eight lines (Data In/Out) are used to send commands from the controller and transfer data back and forth between instruments and the controller.

2. **ATN**—This line (Attention) is operated only by the controller. It specifies whether the information on lines DIO1 - DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages; additionally, every device connected to the bus is required to receive and process every command sent by the controller.

3. **REN**—This line (Remote Enable) controls whether devices on the GPIB are in local or remote modes. In local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed: GPIB originated commands are obeyed, while front panel commands are ignored. The 178 enters the remote state when it receives its listen address (ref: paragraph 3.16.2.1) and REN is enabled. The 178 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LOCAL front panel key is pressed (ref: paragraph 3.16.2.4, item 4).

4. **DAV, NRFD, NDAC**—These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1 -DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to holdup the bus until the slowest device has accepted the information.

5. **EOI**—When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1 - DIO8 is the last byte of a data message. When the 178 receives a data byte with EOI true, the 178 automatically supplies a terminator character (ref: paragraph 3.16.6) following the data byte. When the 178 transmits the last byte of a message (which is always a terminator character), it also sets EOI true.

6. **SRQ**—This line (Service Request) is used by the 178 and other devices on the bus to signal the controller that they request attention. (Ref: paragraph 3.16.5 for 178 Service Request Enable.) Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.

7. **IFC**—This line (Interface Clear) is used by the controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.16.2 Commands

Commands are sent over lines DIO1 - DIO8 with ATN true. They are divided into five classes.

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands

   DCL—Device Clear
   SPE—Serial Poll Enable
   SPD—Serial Poll Disable
   LLO—Local Lockout

5. Addressed Commands

GTL—Go To Local
SDC—Selective Device Clear
GET—Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A and further explanation follows.

3.16.2.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1 -DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes **SP** through **>**). A 32nd address, called unlisten (hexadecimal **3F**, ASCII **?**), is used to command all devices to not read data bytes. The 178 listen address is selected by the rear panel switches, which specify the lower 5 bits of the address. (Ref: table 2-2.) Pressing the front panel ADRS key displays the GPIB address as a decimal device number followed by the ASCII character listen and talk addresses.

3.16.2.2 Talk Address

Talk addresses are used to command a device to transmit data over lines DIO1 - DIO8 whenever ATN is false. There are 31 different available addresses (hexadecimal codes **40** through **5E**, ASCII codes @ through ↑). A 32nd address, called untalk (hexadecimal **5F**, ASCII →) is used to command all devices to cease talking. The lower 5 bits of the 178 talk address are selected by the same rear panel switches used to select the listen address. Thus, if the 178 listen address is hexadecimal **21** (ASCII **!**), the talk address is hexadecimal **41** (ASCII **A**). Pressing the front ADRS key displays the GPIB address as a decimal device number followed by the ASCII character listen and talk addresses.

3.16.2.3 Secondary Address

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the 178.

3.16.2.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the 178 are:

1. **Device Clear (DCL)**—Resets the 178 to the initial power on settings. Refer to table 2-3, step 3 for power on conditions. DCL affects all devices on the bus. This information is also set into the waveform generating circuitry.

2. **Serial Poll Enable (SPE)**—Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to an ASCII blank, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the 178 talk message number 2. When this message is read, the status byte is reset and SRQ released as for the serial poll.

3. **Serial Poll Disable (SPD)**-Discontinues serial poll. Returns instruments to normal talk modes.

4. **Local Lockout (LLO)**—Causes the GPIB interface to enter a state where the front panel LOCAL key is inoperative. Once in this state, the only way to take the interface out of it is to put the REN line in the local state (ref: paragraph 3.16.1, item 3). Local lockout must be sent to the 178 to totally disable front panel modification of the state of the instrument.

3.16.2.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the 178 are:

1. **Go To Local (GTL)**—Commands 178 to go to local mode (ref: paragraph 3.16.1 for explanation to the REN line).

2. **Selective Device Clear (SDC)**—Resets the 178 to initial power on conditions. Refer to paragraph 3.13 for power on conditions. SDC affects only the selected unit.

3. **Group Execute Trigger (GET)**—Causes the actions as specified by the GET mode (**XG**) code (refer to paragraph 3.16.7). If the 178 micro-

proccessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed within 2.5 ms of receipt. Otherwise, it will not be done until current programming is processed.

3.16.3 Data Transfer

In addition to accepting programming characters, the 178 will transmit status information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 64 charactes are received or there is a pause during the transfer of data. At that time, the entire string of received characters is scanned by the microprocessor, which carries out the scan and accepts the next 64 character string. Whenever the microprocessor finished scanning a string, it puts a display on the front panel which reflects the state of input processing at that point. If the EOI line is asserted while sending a character to the 178, the currently programmed terminator character will be put into the input string following the character with the EOI.

3.16.4 Talker

To read a message from the 178, first send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Message Select (**XT**) setting. The last character of the 178's message will be the currently programmed terminator character with the EOI line asserted.

0 Sweep Status. When read: 0 - No sweep.
1 - Sweeping.
1 List of programming errors. When read, message sets to null.
2 Serial poll byte message.
3 Value of most recently programmed selector.
4 Main generator settings.
5 Sweep generator settings.
6 Current marker frequency.
7 Model and software version.

3.16.5 Service Request Enable

XQ followed by its code selects the conditions under which the GPIB SRQ signal will be sent by the 178. The codes are:

0 SRQ off.

1 SRQ sent if a programming error occurred.

3.16.6 End of String or Terminator Specification

XV followed by its argument designates a new End Of String (EOS) or terminator character. The argument is the decimal value of the ASCII character that is to be the new terminator: an EOS character recognized by the 178. Any ASCII character except NUL is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a talk request on the GPIB. During input, it signals, the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to insure that the instrument is in a known state, so that following programming characters will be interpeted correctly.

At power on time, the EOS character is the line feed control character, ASCII character LF (10_{10}). When the 178 issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pullsed low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program **XV**13.

3.16.7 GET Mode

XG followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the 178. The code may be **0, 1** or **−1.**

0 Upon receipt of GET, the programmed waveform values in the scratch pad memory are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (**IJ**) were programmed, except that no error checking is done.

NOTE
Codes 1 and −1 are applicable for Option 001 (stored settings 6 through 245) only.

1 Upon receipt of GET, the stored setting next in sequence after the last stored setting accessed is recalled if it exists. This is the same sequence of events that would occur if an execute, then a trigger action were programmed (**WIJ**) except no error checking is done.

–1 Upon receipt of GET, the stored setting previous in sequence before the last stored setting accessed is recalled if it exists. Then the actions described for code **0** are performed. This is the same sequence of events that would occur if a previous setting, an execute and a trigger action (**U1J**) were programmed, except that no error checking is done.

3.16.8 Local

The front panel LOCAL key switches the GPIB interface to the local mode if it is not locked out (ref: paragraph 3.16.2.4, item 4).

3.16.9 Display

The single quote character (') is used to program a string of characters to be displayed on the front panel display. Program a single quote, the characters to be displayed, followed either by another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 20 characters programmed after the first quote are displayed on the front panel. If fewer than 20 characters are programmed, then blanks are added to fill the display.

Examples (∧ indicates a blank character)

Three programmed inputs

1. '20∧CHARACTER∧LIMIT'
2. 'THIS∧STRING∧IS∧TOO∧LONG∧TO∧DISPLAY∧ENTIRELY'
3. ' '
   (no characters in string)

The Resulting Displays

1. 20∧CHARACTER∧LIMIT∧∧
2. THIS∧STRING∧IS∧TOO∧L
3. (blank display)

3.17 PULSE OPERATION

Model 178 is capable of continuous pulse operation at frequencies up to 100 kHz. In this mode, the sweep generator internally triggers the main generator. Pulse period is set by programming sweep time to any value between 10 μs and 600 sec, with 4 digit or 10 μs resolution (whichever is less). Pulse width equals 1/2f, where f equals the frequency of the main generator from 5 μs to 500,000 sec, with 8 digit resolution. For pulse operation, set up the Model 178 as follows:

Function:	Square Wave
Main Mode:	Triggered
Sweep Mode:	Off
Ext/Int Trigger:	Internal
Sweep Time:	Pulse Period
Frequency:	Reciprocal of two times the pulse width
Amplitude:	Peak-to-peak pulse amplitude
Offset:	As required to set pulse baseline

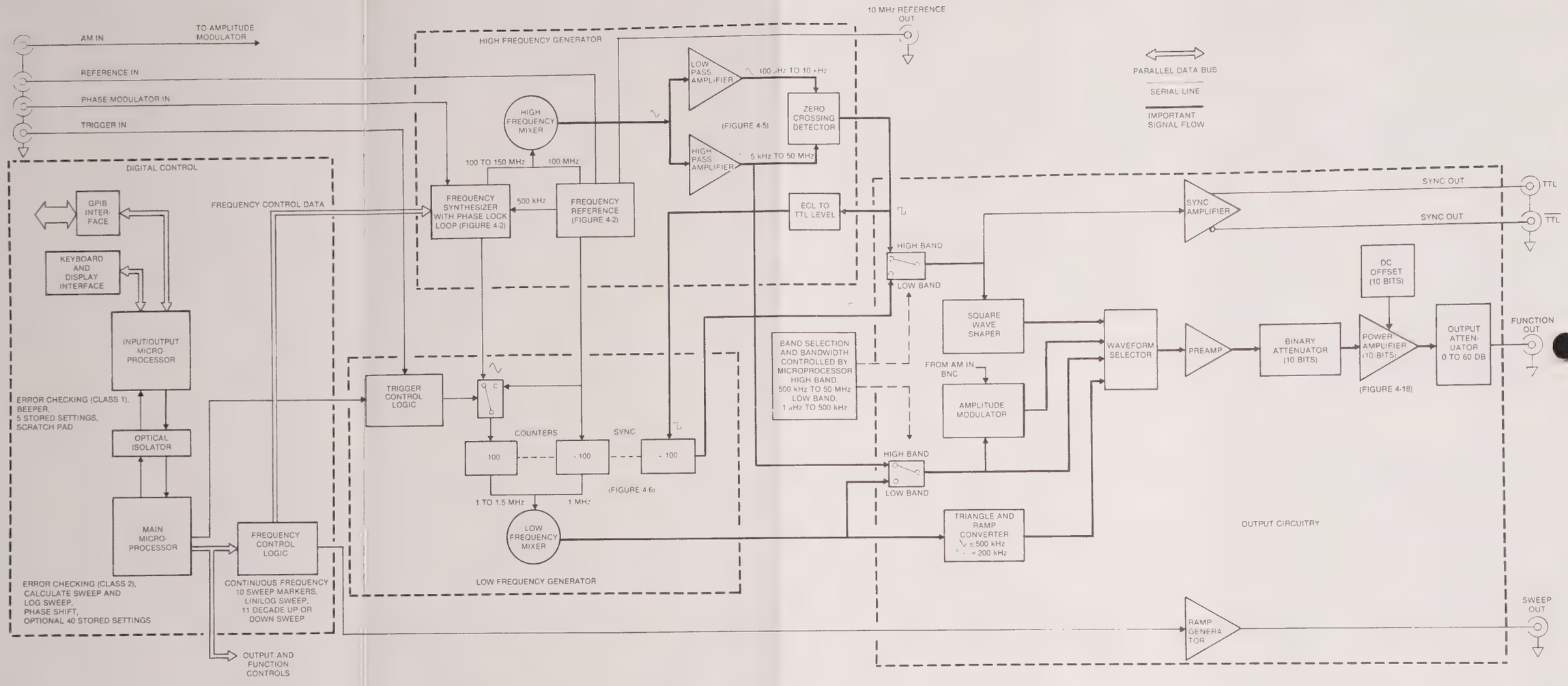


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

Figure 4-1 is the overall functional block diagram. The following paragraphs describe the blocks of the diagram, the overall operation and the functional relationships. Each section will be described in greater detail in subsequent paragraphs.

4.2 GENERAL DESCRIPTION

Model 178 can be divided into four general function groups. These are digital control, high frequency generator, low frequency generator, and output functions.

4.2.1 Digital Control

Two microprocessors control all Model 178 functions. The input/output microprocessor processes external commands from the GPIB and keyboard, detects class 1 errors, provides the scratch pad, five stored settings and beeper, and sends processed input commands to the main microprocessor. This I/O microprocessor also receives data from the main microprocessor and controls the front panel display.

The main microprocessor controls instrument functions, detects class 2 errors, calculates data for log sweep, lin sweep, and phase shift. This main processor also controls the optional 40 stored settings.

The microprocessors communicate on two optically isolated buses. Data is serially transferred between the two microprocessors and free of system grounds because of optical isolation. The main microprocessor communicates with instrument functions by an eight-line parallel bus.

The digital sweep generator is basically an ALU (arithmetic logic unit). The sweep adds numbers to the frequency synthesizer (in a divide-by-N of a phase lock loop) to generate an 11 decade sweep up or down. This digital sweep circuitry also controls the 10 sweep markers, is used with the microprocessor to control log sweep, and sends information to the ramp generator which produces the sweep out signal.

4.2.2 High Frequency Generator

The second major group of functions, the high frequency generator, consists of a phase lock loop with 14 digits of resolution, frequency reference, mixer and pass band amplifiers. The PLL output and reference signal are combined in a high frequency mixer to produce a difference frequency of 100 μHz to 50 MHz. The mixer output signal is amplified by two pass band amplifiers. The high pass amplifier is used for the high frequency output and the low pass amplifier is used for the square wave of the low frequency output. To convert the sine outputs of both pass band amplifiers into a square, a zero crossing detector is used.

4.2.3 Low Frequency Generator

The low frequency generator incorporates three synchronized divide by 100 counters. The synchronization of the counters insures that the sync output will correspond to the zero phase of the selected waveform. Two of the counters divide the synthesizer and reference signal before mixing the signals in a low frequency mixer. The low frequency output is used as a sine wave output (1 μHz to 500 kHz). The third divide by 100 counter is used to scale the low frequency square from the zero crossing detector to the same frequency range as the low frequency sine.

The two output bands of frequencies are available to the output, one directly from the frequency synthesizer and one from the low frequency generator. The microprocessor switches from low frequency generator to high frequency when a frequency is selected from 501 kHz and above.

In sweep mode the wide pass band of the high pass amplifier (5 kHz to 50 MHz) is used to obtain the 11 decade sweep.

Associated with the low frequency generator is the trigger control logic. This circuitry allows the low frequency generator to be triggered.

4.2.4 Output

The output circuit contains bandpass switches, waveform selection circuitry preamp, attenuators and power amplifier. The main microprocessor controls all these functions to give the correct signal with optimized waveform quality at the programmed value and dc offset.

NOTE

Detailed analysis will begin with the frequency synthesizer section, the high and low frequency generator section, the output circuits and, finally, the microprocessor section. Schematics, component location drawings and parts lists are in section 7.

4.3 FREQUENCY REFERENCE AND SYNTHESIZER LOOP

Figure 4-2 shows an expanded block diagram of the frequency reference and frequency synthesizer of the high frequency generator. The purpose of these functions is to 1) supply all internal reference signals and 2) supply a phase locked loop output signal with 14 digits of resolution.

4.3.1 Frequency Reference

The reference generator is shown in two parts, the frequency reference, and the reference phase lock loop. Refer to figure 4-2 and the Reference Board schematic while reading this discussion.

The heart of the frequency reference generator is the 10 MHz crystal oscillator Y1 and Q1 (sheet 1). The high impedance output of this oscillator drives buffer Q2 which feeds Nor gate U9-5. The output at U9-10 is fed to the 10 MHz REF OUT BNC and through dividers U8, U6, and buffer Q3 to generate the 500 kHz reference for the phase lock loop.

A 10 MHz signal from the oscillator is also fed through U9-1 to produce the 100 MHz signal required for the high and low mixers. The square pulses of U9-1 are turned into positive spikes via C34 and CR12. These spikes drive the tuned tank of Q4's gate. Q4's output is capacitor coupled to L4, C45, and C46, which is tuned to resonate at the fifth harmonic. The tank's output is fed to U4 where the sine is converted into an ECL signal rich in harmonic content. The second harmonic, 100 MHz, is passed through the L network C52 and L2 for high pass filtering and into tank circuit L5, C53, and C54. ECL output of the 100 MHz signal is buffered via Q6 and associated circuitry.

The reference phase lock loop provides internal or external synchronization of the Y1/Q1 oscillator. A temperature compensated, 10 MHz crystal oscillator (Y2 on sheet 2), internally synchronizes the Y1 oscillator, thereby providing greater frequency stability. If Option 002 is installed, the Y2 oscillator is replaced with an even more stable oscillator. If a 1 to 10 MHz (at 1 MHz multiples) sine or pulse signal of 0.5 to 10Vp-p is injected at the rear panel "REF IN" connector, it automatically replaces the signal from Y2.

External input signals are shaped and amplitude limited by CR10 and CR11, then fed to zero crossing detector U5, which converts the input signal to a TTL level. The combination of U1 and U6 make up a 930ns one-shot that samples the signal at a 1 MHz rate. Since the sampling rate is somewhat fixed, the system will not lock to the input signal unless it is within ± 5 ppm of a multiple of 1 MHz. With the proper input signal present, the one-shot generates a 1 MHz pulse at U6-5 (driving U11-9 on sheet 2), and brings U1-13 high. Inverter U7 forces E12 (and therefore U11-2 and 12 on sheet 2) low. The 1 MHz signal at U10-9 (originating from TCXO, Y2) is blocked because U11-3 is forced high. With a low at U11-11, the signal from E14 is twice inverted, first at pin 8, then again at pin 6, where it becomes the phase detector reference input (U2-3 sheet 1).

If no signal is present at the "REF IN" connector, U1-13 is low and U7-8 (E12 on sheet 1 and E15 on sheet 2) is high. U11-11 (sheet 2) is low, causing U11-8 to be high, blocking any signal that may be present at E14. The 10 MHz crystal oscillator output from Y2-8 is divided by U10, then inverted at U11-3 and 6.

This signal (originating either internally or externally) is input to U2-3 (sheet 1) and is compared with a second 1 MHz signal at U2-1. This second signal comes from the reference oscillator, Y1/Q1, after being divided by U8, and buffered by U7 pins 3, 4 and 13. Frequency adjustment is then made as in any phase lock loop.

The phase comparator converts a phase difference of the two inputs into two spikes. To help reduce noise, the 4044's internal charge pump is not used. Instead a charge pump of CR1, CR2, CR3 and CR4 receives the two spikes from pins 13 and 2 to generate a positive or negative current input to U3 pin 2. The active low pass filter then produces the needed dc level to control the capacitance of varactor CR7 which adjusts the frequency and phase of the crystal.

If the reference is too far away from a 1 MHz multiple, no reference will be felt at U2 pin 3. U1 with input pins 9 and 10 monitors U2's output. With no reference, U1 pin 5 goes high. This high is felt via E2 to the microprocessor, which will display "REFERENCE NOT LOCKED".

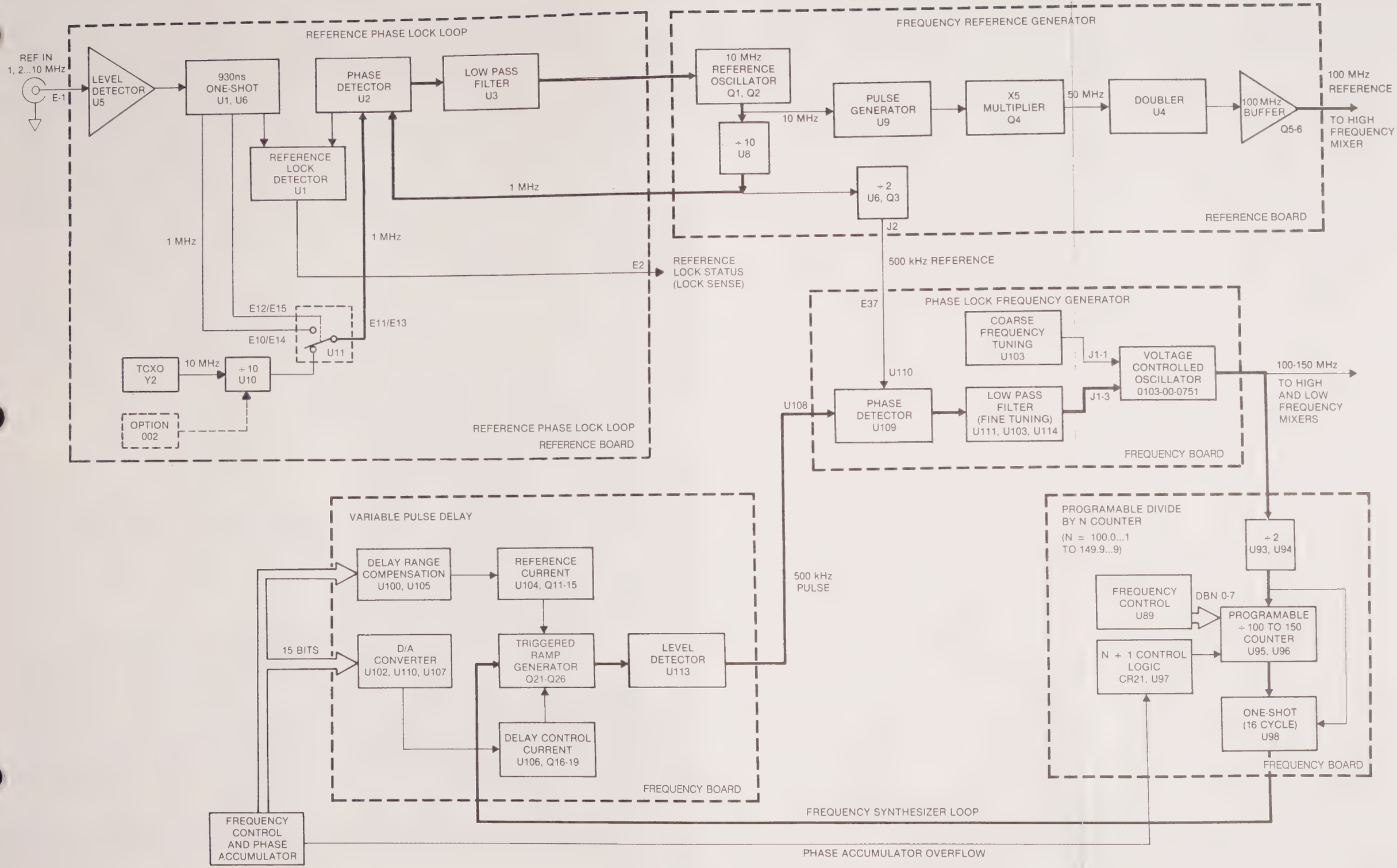


Figure 4-2. Frequency Reference and Synthesizer Loop Diagram

4.3.2 Frequency Synthesizer Loop

As shown on figure 4-2, the frequency synthesizer loop consists of three major blocks (phase lock frequency generator, programmable divide-by-N counter, variable pulse delay) plus the phase accumulator. The phase lock frequency generator block is standard configuration with its phase detector, active low pass filter, and VCO. However, the divide-by-N in the PLL feedback is unique. The purpose of the divide-by-N block, variable pulse delay block, and phase accumulator is to produce a synthesized frequency of 14 digits. Discussion will begin with the basic loop and then develop the theory of the high resolution divide-by-N circuitry.

4.3.2.1 Phase Lock Frequency Generator

Refer to the Frequency Board schematic sheet 5 and figure 4-2 while reading this discussion. The phase detector, U109, is an ECL integrated chip with much faster switching speed and much less noise than the MC4044 as used in the external reference phase lock loop. This integrated circuit receives a 500 kHz signal from the reference board and a 500 kHz signal from the pulse delay circuitry. CR15, CR16, CR17, and CR18 change the spiking output of U109 into a positive or negative current which feeds the active low pass filters (U111 pin 2).

The low pass filter produces a DC voltage that is fed to U103 for coarse VCO tuning and U114 for fine tuning of the VCO.

Now refer to the VCO Board schematic. The VCO (voltage controlled oscillator is a quarter wave transmission line type. The quarter wave network is used as a reactance transformer which converts the capacitive reactance of the varactor diodes to a high Q inductive reactance. For the band width of approximately 100 to 150 MHz, this circuit acts like a tank circuit with a very high Q and low spurious noise. Q1 is a linear amplifier whose function is to furnish replenishing energy to the oscillator. Output to buffering transistor Q2 is accomplished by coupling from Q1's drain via C10 and sending through low pass pi filter (C12, C13, and L4). The output is then fed to the divide-by-2, divide-by-N and to the high frequency mixer.

4.3.2.2 Divide-by-N Theory

Unlike the conventional phase lock loop, this divide-by-N counter divides by 3 digits plus an 11-digit fraction. This gives the VCO frequency 14 digits of resolution. The excessive spurious frequencies involved are eliminated by a pulse delay circuit.

A typical PLL will have a relationship of reference frequency equals the VCO divided by prescaler divided by the number N. For example, if a VCO frequency of 25 MHz is assumed and a 500 kHz reference is assumed, then N will equal 25 and the prescaler must equal 2 to give the proper reference.

$$\frac{25\text{MHz}}{25\ (2)} = 500\ \text{kHz}$$

The same relationship exists for the 178 PLL except N includes a fractional part (N becomes N.F). Hence, for a VCO frequency of 120.14956 MHz, and an assumed 500 kHz reference, then N.F equals 120.14956 (a whole number plus a fraction), and the prescaler must equal 2 to give the proper reference.

$$\frac{120.14956\ \text{MHz}}{120.14954(2)} = 500\ \text{kHz}$$

or,

$$\frac{f_{VCO}}{(\text{N.F})(\text{Prescaler})} = \text{Reference}$$

The means for obtaining a divide by N.F where F is a fractional part can be accomplished by averaging two whole numbers. The question arises then, for example, how would one average two numbers such as 130 and 131 to obtain 130.25? Expressed in mathematical terms:

$$130.25 = \frac{3(130) + 1(131)}{(3+1)}$$

Where 3 is the number of 130's that must be added to one 131 to obtain an average of 130.25.

The 178 PLL circuit includes a phase accumulator whose purpose is to cause the programable divide-by-N.F of the PLL to divide by N (a whole number) and at the correct moment divide by N + 1. The phase accumulator also causes the pulse delay to average the two different divisors so that an average divide by N.F (a whole number plus a fraction) will produce 500 kHz, which is equal to the 500 kHz of the reference frequency at the PLL phase detector.

For example, refer to figure 4-3. Assume the VCO frequency to be 130.25 MHz. The reference is 500 kHz and the prescaler is divide-by-2. This results in a fre-

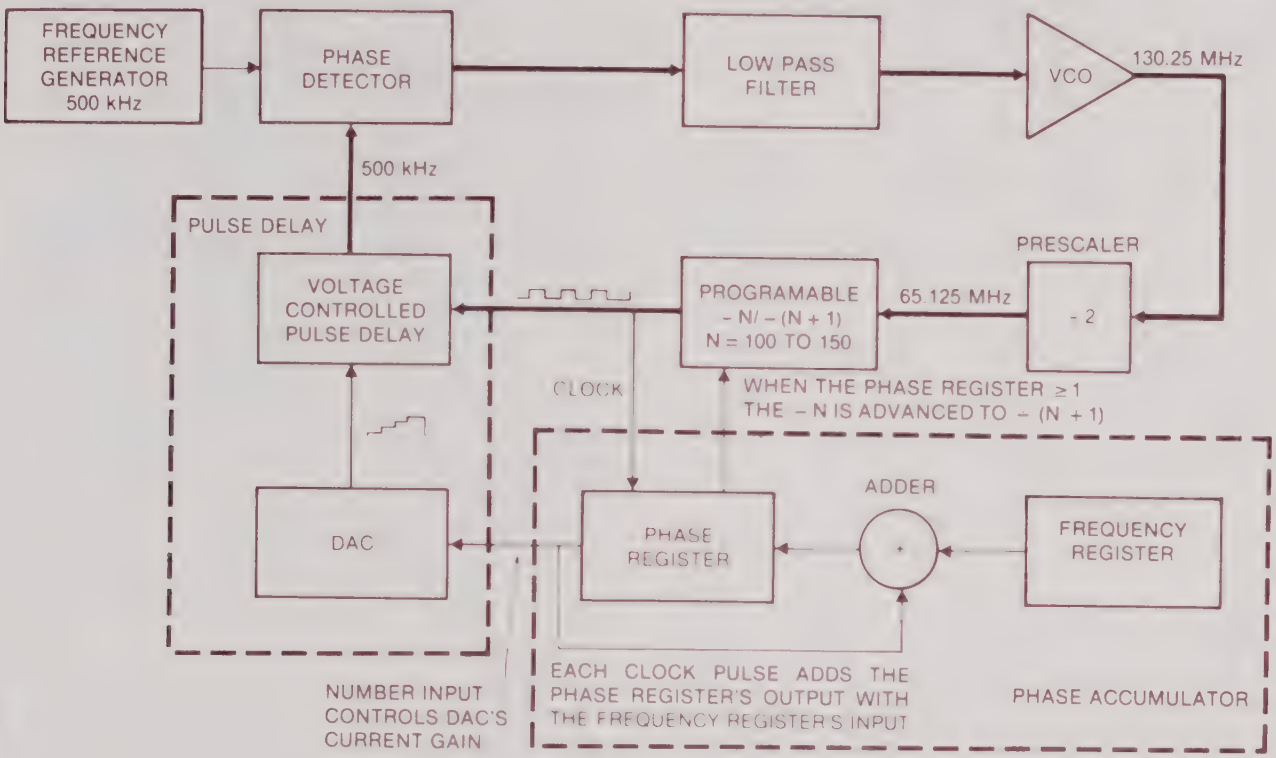


Figure 4-3. PLL with ÷ N and ÷ (N + 1)

quency of 65.125 MHz coming from the prescaler and going into the divide by N counter. N = 130 and N + 1 = 131. Keep in mind that it is the divisors (N and N + 1) that will be averaged to produce the ÷ 130.25 divisor required to feed the 500 kHz to the phase detector.

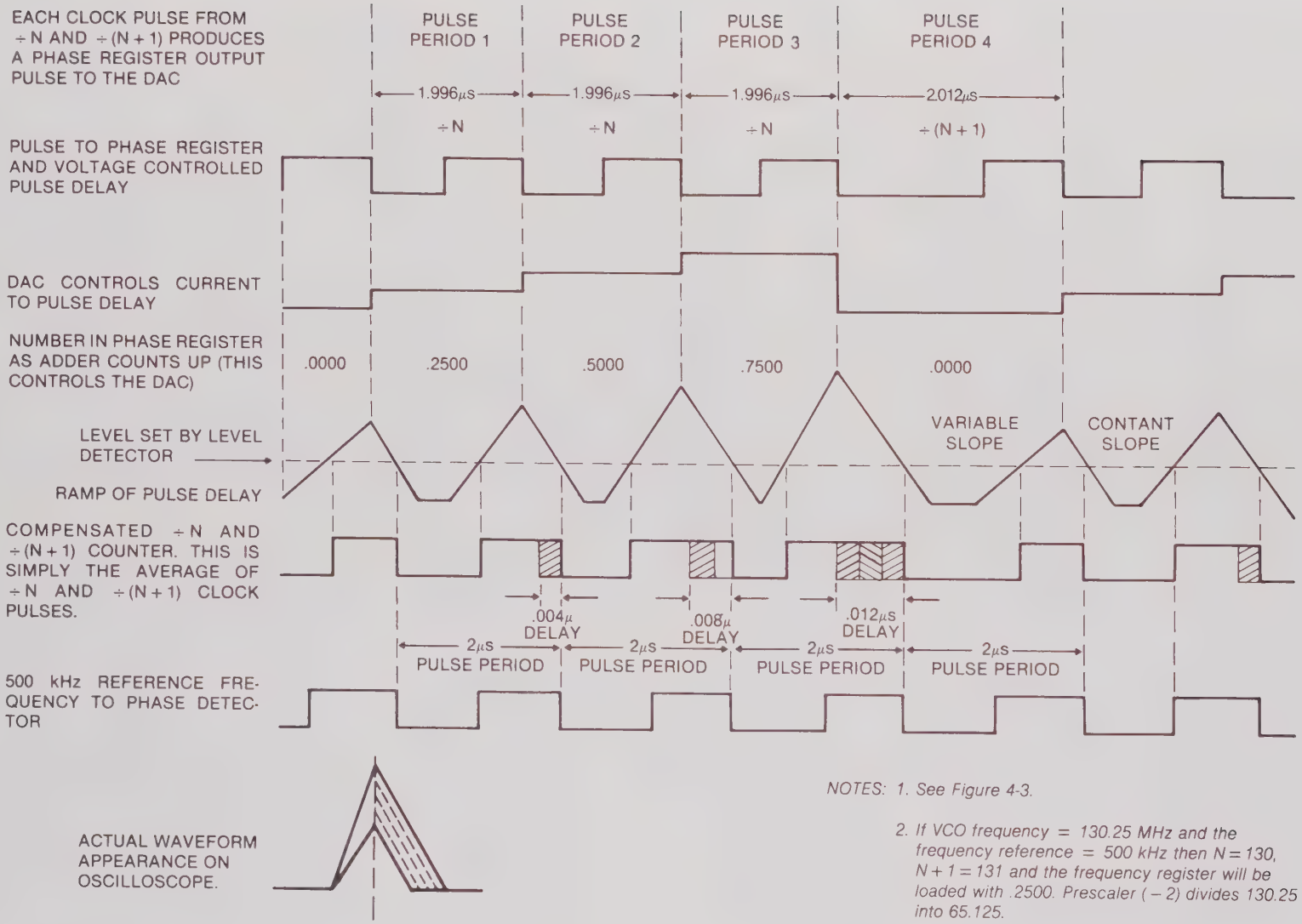
The 65.125 MHz from the prescaler divided by 130 = 500.96 kHz or a single pulse period of 1.996 μs. To obtain the desired 130.25 divisor, only 3 pulse periods are needed at this frequency. The fourth pulse period needs to be 2.012 μs: 3(1.996 μs pulse periods) plus 1 (2.012 μs pulse period) gives an average of four 2 μs pulse periods giving the required 500 kHz frequency rate. Conveniently, a 2.012 μs pulse period is a single pulse period of 65.125 MHz divided by 131. This technique of division gives a jittery output as the frequency is divided by N of the pulse for three cycles and then divided by N + 1 for one cycle. Thus, a smoothing or averaging of the pulse periods is needed.

Now refer to both figure 4-3 and 4-4. Assume the phase register is at 0.2500 for the first 1.99 μs pulse period. The first pulse from the ÷ N is fed to two places. The pulse's positive leading edge causes a ramp in the pulse delay to charge. Since the output of the phase register is fed into the DAC of the pulse delay. the charging ramp current will be greater than the previous pulse period. This higher peak triangle (ramp or pulse delay) causes a 0.004 μs delay on the trailing edge of the pulse delay circuit. The trailing edge to the edge triggered phase detector makes the detector see a 2 μs pulse period or a 500 kHz frequency rate.

The first pulse is also fed to the phase register. Here the trailing edge of the first 1.996 μs pulse causes the phase register with 0.2500 of the phase register's output. A new number, 0.5000 is now stored in the phase register.

For pulse period 2, the ramp charges higher than pulse period 1 because the DAC has a larger number controlling its current output. This larger ramp results in an 0.008 μs delay. Hence the second compensated pulse period = 2 μs also.

The trailing edge of pulse period 2 again causes the output of the phase register to be added with the 0.2500 of



NOTES: 1. See Figure 4-3.

2. If VCO frequency = 130.25 MHz and the frequency reference = 500 kHz then N = 130, N + 1 = 131 and the frequency register will be loaded with .2500. Prescaler (– 2) divides 130.25 into 65.125.

3. This example is extremely exaggerated. Actual delay for this frequency would be approximately .0004% of the uncompensated pulse width to a maximum of .00012% with maximum compensation.

Figure 4-4. Example of ÷N and ÷(N +1)

the frequency register for a new phase register number of 0.7500.

Pulse period 3 is excactly the same as the previous 2 pulse periods except pulse period 3 delays the pulse by 0.012 μs and the trailing edge causes the phase register to add up to 1. Whenever the phase register goes to 1 or greater, the one is carried to the divide-by-N. The programmable divide-by-N then divide divides by N + 1. Any remainder stays within the phase register for addition on the next new cycle. Thus, with the divide by N + 1, pulse period 4 becomes 2.012 μs long, the 0.0000 remains in the phase register, and a new 8.000 μs cycle pulse period averaging begins.

There are three important facts about the example presented. First, the positive part of the pulse is always the same width for both the N and N + 1 pulse period length. That is, if the positive pulse of 1.996 μs pulse is 50% duty cycle or 0.998 μs in width, the positive pulse for the 2.012 μs pulse will also be 0.998 μs in width or 49.6% of the duty cycle.

Second, figure 4-4 as drawn is very exaggerated. On a scope one would observe a trailing edge of constant duration and height that appears constant. The leading edge, however, would be blurred.

Third, for a complex number such as 20.139468 would yield a divide by N to divide by N + 1 ratio of about 6.1701035 pulse periods to 1. Hence 10,000,000 pulse periods may need to pass before the cycle wil repeat (if ever). The fractional remainder in the phase register of each carry over will vary tremendously with a number requiring that many pulse periods.

4.3.2.3 Divide-by-N Description

Now refer to the Frequency Board schematic sheet 5 and figure 4-2. U94 is the divide-by-2 prescaler. The output pin 3 will always be from 50 to 75 MHz. U95 and U96 make up the programmable divide-by-N and N + 1. The outputs of each chip are tied together into a wired OR function. The overflow from the phase accumulator is fed into the OVERFLOW line to CR21 and U97 which causes the counter to add 1 to the divide-by-N at the appropriate moments.

The jittering 500 kHz output of the programmable divide-by-N flows from U94-14 to U98-5, 6, 11, 12. The positive pulse is made into a precise width by running the pulse through U98. U98 functions as a one-shot. U98 takes the positive edge of a 500 kHz pulse and holds the pulse for only 16 counts of prescaled N.F VCO frequency rate. This prescaled N.F VCO frequency is fed into U98-13.

The resulting pulse output is fed to U99. From here the "pulse delay inputs" are fed to the bases of Q24 and Q25 on page 7-24 Q25's collector output is coupled to the base of Q27. Q27's output controls the bridge diodes CR28, CR29, CR30 and CR31 which serve as an integrator

Current sources for the integrator come from U104 and associated circuitry and U106 with associated circuitry. The gain of the reset current (U104 and circuitry) is controlled by DAC U102. The charge current is controlled by DAC U101. DAC U100 controls the high frequency spur compensation (U105) which increases the charging current as the frequency reaches the upper range.

The resulting dual sloped ramp of the charging and reset current with bridge diodes and C105, is amplified via U112, Q20 through Q23 and Q26. From here the ramp is converted into a pulse via the level detector U113. As discussed earlier, the trailing edge of the average pulse is then fed to comparator U109 on sheet 5.

Action of the phase accumulator will be described in the digital ramp generator section.

4.4 MIXING SYSTEMS AND SQUARE/SYNC CIRCUITS

There are two frequency mixers, a high and low mixer (figure 4-1). Associated with the high frequency mixer is the sine wave *microprocessor controlled band width* of 500 kHz to 50 MHz, and the entire square wave band width. The low frequency mixer produces the sine and triangle *microprocessor controlled bandwidths* of 1μHz to 500 kHz, and, in addition, provides for synthesized triggering.

Discussion will begin with the high frequency mixer, progress to the square/sync generator and then the low frequency generator which includes the low frequency mixer and the low frequency square output of the high frequency mixer.

4.4.1 High Frequency Mixer

Refer to figure 4-5 and the Frequency Board schematic sheet 7. The purpose of the high frequency mixer is to

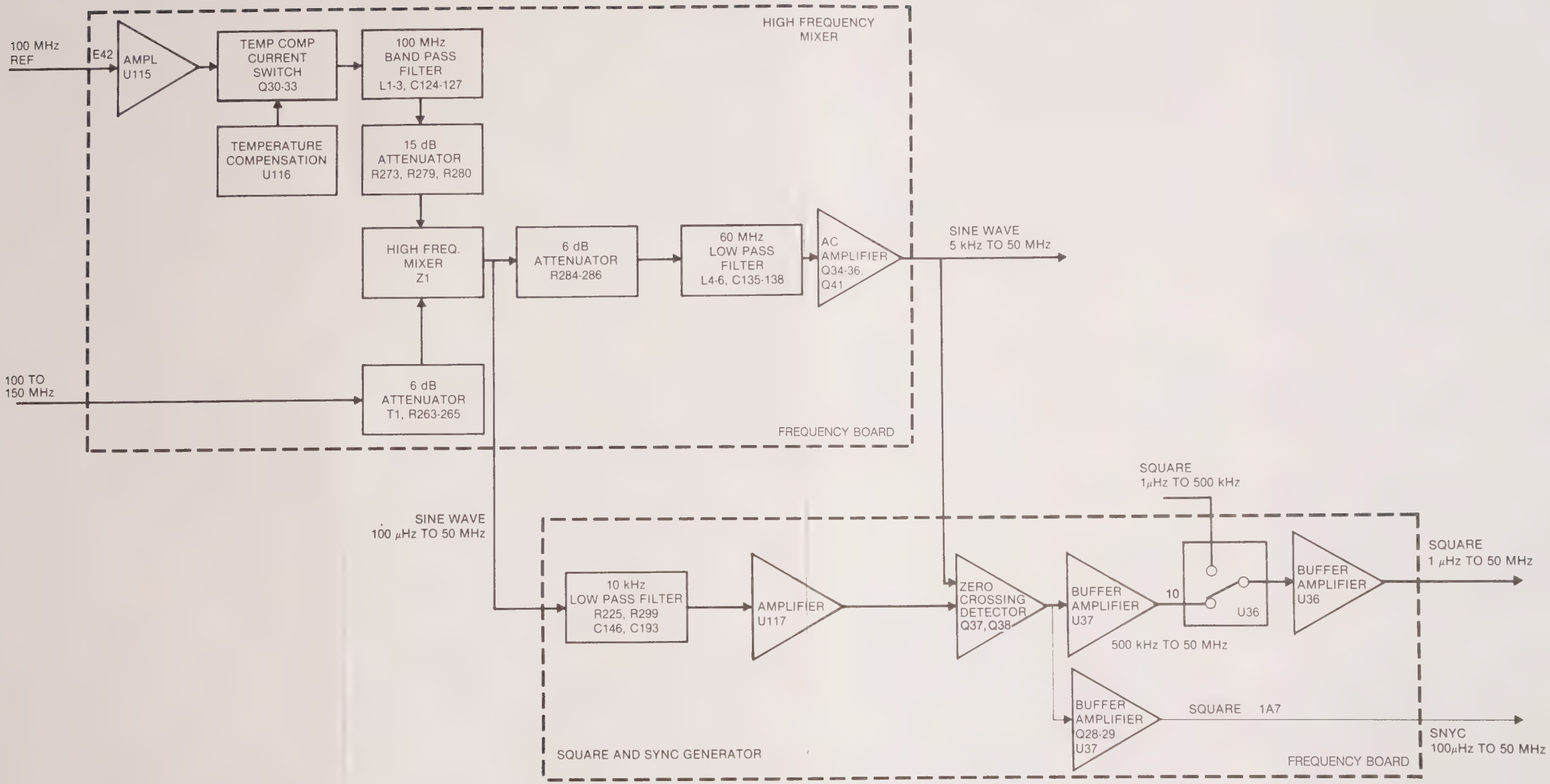

HIGH FREQUENCY MIXER
100 MHz REF
E42
AMPL U115
TEMP COMP CURRENT SWITCH Q30-33
100 MHz BAND PASS FILTER L1-3, C124-127
TEMPERATURE COMPENSATION U116
15 dB ATTENUATOR R273, R279, R280
HIGH FREQ. MIXER Z1
6 dB ATTENUATOR R284-286
60 MHz LOW PASS FILTER L4-6, C135-138
AC AMPLIFIER Q34-36, Q41
SINE WAVE 5 kHz TO 50 MHz
100 TO 150 MHz
6 dB ATTENUATOR T1, R263-265
FREQUENCY BOARD
SQUARE 1μHz TO 500 kHz
SINE WAVE 100 μHz TO 50 MHz
10 kHz LOW PASS FILTER R225, R299 C146, C193
AMPLIFIER U117
ZERO CROSSING DETECTOR Q37, Q38
BUFFER AMPLIFIER U37
10
U36
500 kHz TO 50 MHz
BUFFER AMPLIFIER U36
SQUARE 1 μHz TO 50 MHz
BUFFER AMPLIFIER Q28-29 U37
SQUARE 1A7
SNYC 100μHz TO 50 MHz
SQUARE AND SYNC GENERATOR
FREQUENCY BOARD

Figure 4-5. Mixer and Square Wave Block Diagram

heterodyne the 100 MHz reference and the synthesizer VCO frequency of 100 to 150 MHz. The difference frequency of 100μHz to 50 MHz is routed to high pass and low passband amplifier circuits.

Tracing from the 100 MHz reference, the 100 MHz signal is fed into amplifier U115-5. Here the reference is converted to an ECL square wave whose output drives the differential current switch of Q32 and Q33 Current for the switch is supplied by a constant current source Q30 and Q31. U116 and CR33 control Q30 and Q31 for temperature compensation.

The switching action of Q32 and Q33 amplifies the ECL signal from U115. The signal is then passed on to the 100 MHz filter L1-L3 and C124-C127 to obtain a very pure sine wave. The sine wave is applied to pin 1 of mixer Z1 through a 15dB attenuator consisting of R273, R279, and R280. The 15dB attenuator insures mixer Z1 will operate within its most linear range.

The VCO frequency, 100 to 150 MHz, is fed into the mixer via a 6dB attenuator to insure the best possible output for mixer Z1. The VCO attenuator consists of T1, R263-R265.

The mixer's output signal of 100μHz to 50 MHz is sent through a high frequency and a low frequency path. The high frequency path is through a 6dB attenuator R284-R286 and the 60 MHz low pass pi filter networks consisting of L4-L6 and C135-138. The three stage ac amplifier Q34-Q36 and Q39-Q41, amplifies a pass band of 5 kHz to 50 MHz by 32 dB. At the output of this high frequency amplifier, the sine wave goes to the function output selector via relay K1 for 500 kHz and up and to the zero crossing detector for square conversion.

The low frequency path from mixer Z1 is through R295, R299, and filter capacitors C146 and C193. After the signal of 100 μHz to 10 kHz is amplified by U117, the signal is directed to the zero crossing detector for square conversion.

4.4.2 Square and Sync Generator

Since the high frequency mixer produces a full frequency range of sine wave, the purpose of the zero crossing detector is to convert the sine into a full frequency range of square. The detector also synchronizes the upper frequency band of sine wave with the square and TTL out, while the low frequency generator synchronizes the low band of square and TTL.

The differential pair Q37 and Q38 are called a zero crossing detector because the two levels of square are only produced when a sine wave input crosses a 0 Vdc detector level.

For example, if a sine wave 500 kHz to 50 MHz is selected, relay K1 will be on and the sine wave will be connected to the output circuitry. Q37 will be a zero volt reference to Q38 because the low pass amplifier of 100μHz to 10 kHz will be out of range. When a pass band is out of range, it acts essentially as 0V reference to one of the transistors in the differential pair. Thus with a 0V reference on Q37, Q38 will produce an ECL square which will be fed to pin 9 of U37. From U37-2, the signal is fed to U36 (Frequency Board schematic sheet 2). U36 is a buffer and microprocessor controlled switch that selects either the divide-by-100 square of the low frequency generator or the high frequency square. In this example, U36 will send a square signal that will eventually become the squarewave and TTL sine signal which will be synchronous to the sine wave out.

For a signal below 500 kHz, either Q38 or Q37 will be a zero reference depending on which pass band amplifier is out of range. The resulting square wave of Q38, Q37 and U37 will be fed from U37 pins 5 and 7 to another line buffer of U37 which feeds Q28 and Q29. The purpose of Q28 and Q29 is to translate an ECL level signal of 100 μHz-to-50 MHz into a TTL level. The TTL signal from the collector of Q29 is fed to one divide-by-100 counter of the low frequency generator. This signal is synchronized with the other two divide-by-100 counters of the low frequency generator to insure the low frequency sine will be synchronized with the square before the square is fed on to become a TTL out and square out.

Further discussion of U36 and square shaping output signals will be made after discussion of the low frequency generator.

4.5 LOW FREQUENCY GENERATOR

The purpose of the low frequency generator (figure 4-1) is to produce the low band of frequencies 1 μHz to 500 kHz for sine and square. To accomplish this, the low frequency generator uses the square signal from the high frequency mixer plus utlilzes the low frequency mixer to generate the required sine band width. Production of the sine and square in this manner requires some digital circuitry to insure synchronization of the waveforms.

In addition to these characteristics the low frequency generator can be triggered internally or externally for single or gated waveforms.

Now refer to figure 4-6. The low frequency generator discussion will first develop the three synchronized divide-by-100 counters the triggered baseline, a low frequency mixer, and finally the trigger input and control section.

4.5.1 Three Divide-by-100 Counters

One divide-by-100 counter divides the 100 μHz to 50 MHz square from the high frequency mixer. The other two divide-by-100 counters are used to divide the 100 MHz reference and the 100 to 150 MHz VCO frequency for the low frequency mixer. These two counters also synchronize the square divide-by-100 counter so that the low frequency square and sine will be in phase.

Beginning with the 100μHz to 50 MHz square signal counter, the signal from the collector of Q29 (Frequency Board schematic sheet 7) is applied to U27-12 on sheet 1 coordinates A7. From here the signal is divided by 5 via U27, U21, and U20, divided by 10 via U23, and divided by 2 via U11. Nand gates U19 switch the divide-by-2 counter out of the circuit whenever ramp is selected. Hence the counter becomes a divide-by-50 for ramp only. The output of U19 is fed to high/low band switch U27 and to a counter of the trigger control circuits.

Now refer to the Frequency Board schematic sheet 2 and figure 4-6. Both divide-by-100 counters for the low frequency mixer are grouped into divide-by-5, divide-by-5 and divide-by-4 circuits. The variable counter inputs are controlled by trigger switch U28, U31 and U32, which will be discussed in the trigger input and control logic.

The 100 MHz reference is divided by 5 via U29 and U30, divided by 5 via U25 and U24 and translated from ECL to TTL at U118 pin 2. The 4 MHz TTL is sent to U1 via buffer U18 on Frequency Board schematic sheet 1, coordinates C7. Here the signal is divided by 4. The resulting 1 MHz signal is sent through the trigger baseline selection U18-2 (coordinates A2) to the low frequency mixer. The 1 MHz reference is also sent to the digital mixer U11-14 for counter synchronization.

The path of the 100 to 150 MHz VCO (Frequency Board schematic sheet 2) is through a divide-by-5 via U32 and U33, divide-by-5 via U26 and U24, and through U118 to translate the ECL level into a TTL level. From U118 pin 2, the signal is sent to U3 on the Frequency Board schematic sheet 1. U3 is a divide-by-4 with four different phase outputs of 0°, 90°, 180°, 270°. The different phases are used for triggering purposes. Outputs from U3 are fed through the trigger baseline selector U4 to the low frequency generator. U3-9 output also feeds to U11-12, the clock input to the digital mixer.

4.5.2 Synchronization of the Low Frequency Sine and Square Counters

Since the same 1 MHz reference and 1 to 1.5 MHz VCO signals are sent to both the low frequency mixer and digital mixer, outputs from both mixers will be in phase. By using the output of the digital mixer to sync the low frequency square, the square wave will be clean plus the waveforms will be synchronized.

The output from the digital mixer U11 is produced by using the trailing edge of the 1 to 1.5 MHz clock pulse at U11-12 to sample a 1 MHz pulse width into U11-14. This technique produces a clock pulse output at U11-10 equal to the difference frequency.

The difference frequency from U11-10 is one of three signals used to monitor the sync relationship between the low frequency mixer and the divide-by-100 of the square. Tracing the ouput of the digital mixer U11-10, the signal flows through U12 pins 8, 10, 3, 2, 6, 5, 1 and 4 to Nand gates U13 pins 9 and 5.

The other two signals for monitoring the sync come from the divide-by-100 counter of the square. One signal comes from the output of U11-7 to one-shot U10 and U13. The one-shot is used to limit the negative pulse width, which is fed to U13-11 and 4.

The third signal comes from the divide-by-5, divide-by-10, and the divide-by-2 that make up the divide-by-100 counter. These inputs are fed to U22-1, 2, 4, 5. From U22 a signal is sent to U20 and then to U13 pins 10 and 3.

The three paths feeding U13-11, 10, 9, 3, 4, and 5 will cause U13 pins 6 and 8 to go low if the mixer frequency is not within 1μs of the sync or if the proper comparisons are not made on count 0 and 99 of the low frequency square. If U13 pins 8 and 6 are forced to go low, the divide-by-100 counter will be reset to start the count in phase with the digital mixer output. If the counter is synchronized, U13 pins 8 and 6 will remain disabled from the circuit. (Ref: figure 4-7.)

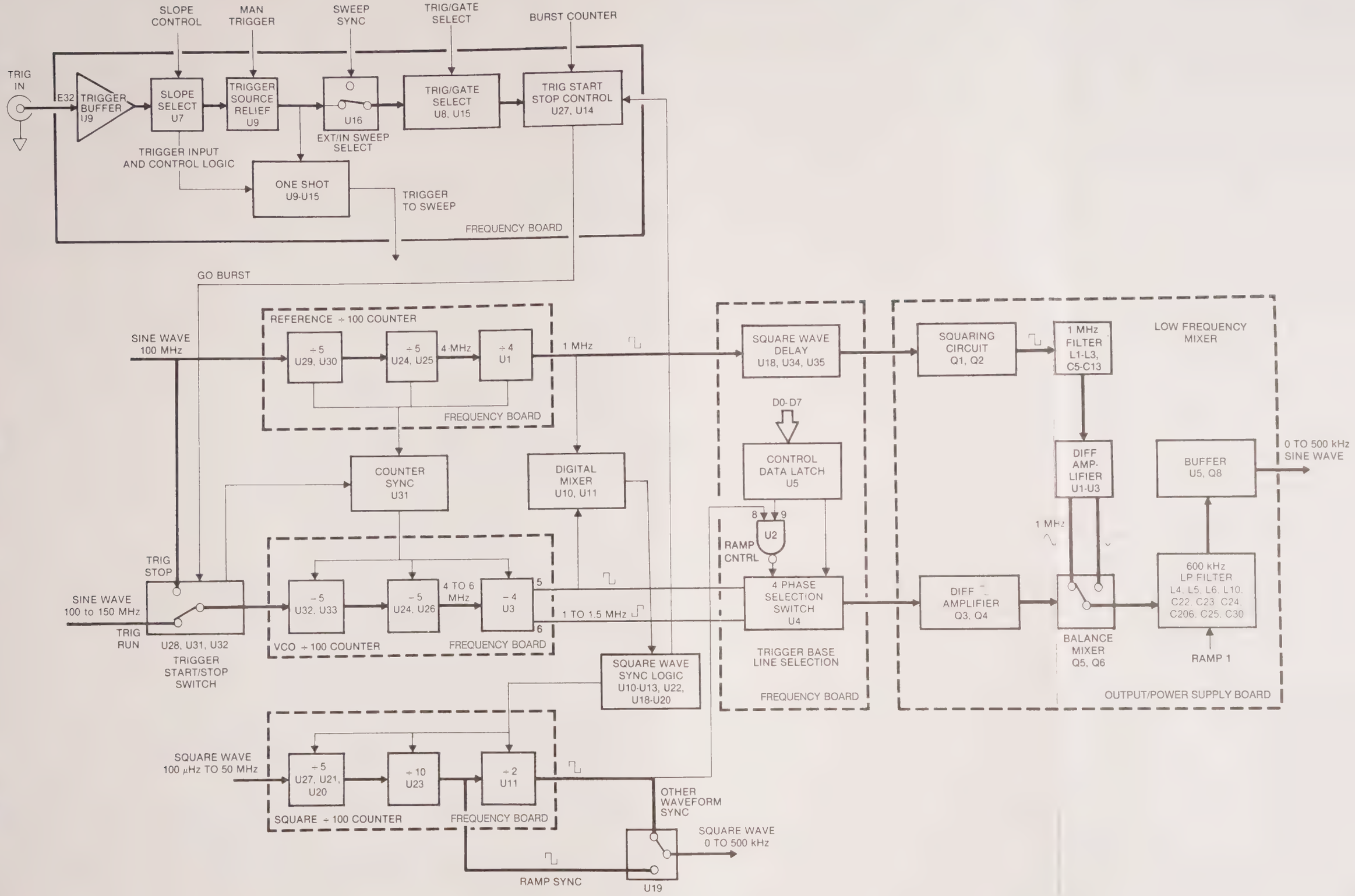


Figure 4-6. Low Frequency Generator Block Diagram

TEST CONDITIONS: RESET PROGRAM MODE (MAIN) TO GATED, FREQUENCY TO 100 kHz AND SUPPLY 15 kHz TO TRIG IN.

U18-8	4 MHz TTL
U10-1	1 MHz TTL
U10-13	1 MHz TTL
U11-10	High TTL

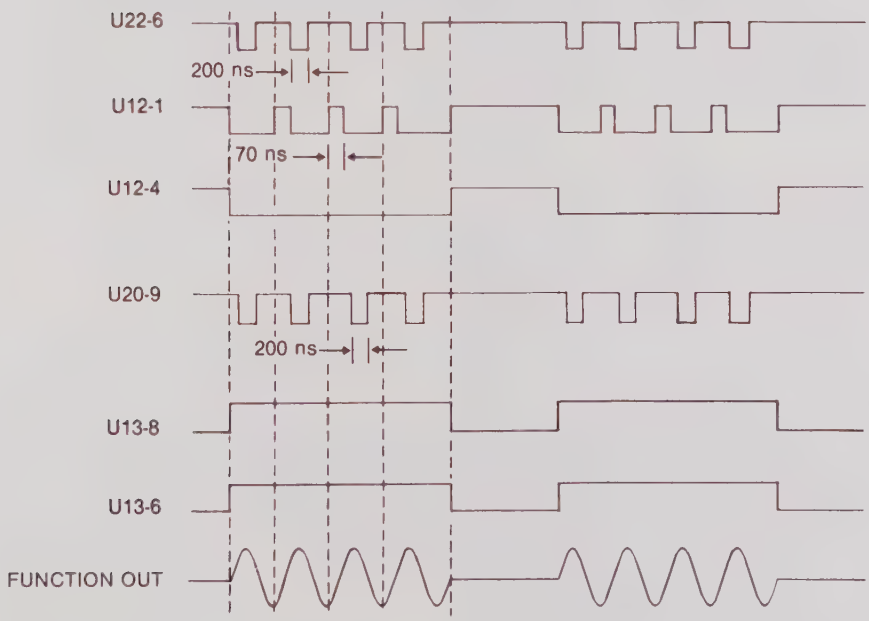


Figure 4-7. Square Wave Sync Logic (Ref: Frequency Board Schematic Sheet 1)

4.5.3 Trigger Base Line Selection

The trigger base line selection is used in trigger and gated modes. Since the 1 MHz reference and the 1 to 1.5 MHz VCO must pass through the baseline selection before being mixed in the low frequency mixer, a brief description is given here and greater development given in the trigger section.

The trigger baseline selection block (figure 4-6 and Frequency Board schematic sheet 1) has two functions: first, to set the baseline in triggered modes, and second, to select the symmetry when a ramp is selected.

The 1 MHz reference square wave from U1 is applied to the square wave delay U18, U35, and U34. U35 is a one-shot whose pulse width is varied to compensate for fixed delays in the low frequency generator. U35 feeds U34 whose output pulse drives the squaring circuit of the frequency mixer section.

The 1 to 1.5 MHz VCO from counter U3-5, 6, 8, 9 has four different phases of output. These phases are fed into the phase selection switch U4. U4 is controlled by the data latch U5, which decodes the microprocessor data. Thus, output from U4-5 will be one of the four phases sent to U4, which will determine the trigger baseline in the trigger modes or the symmetry when a ramp is selected. Output of U4-5 is fed to CR3 on the Output/Power Supply schematic sheet 1.

4.5.4 Low Frequency Mixer

The low frequency mixer heterodynes the 1 MHz reference and the 1 to 1.5 MHz variable frequencies to produce the 1 μHz to 500 kHz ouput frequencies. Refer to the Output/Power Supply schematic sheet 1 and figure 4-6. The low frequency mixer block receives two inputs: the 1 MHz reference square wave from the square wave delay circuit and the 1 to 1.5 MHz square wave from the four phase selection switch.

The 1 MHz reference from the square wave (of the Frequency Board schematic sheet 1) delay circuit drives a squaring circuit Q1 and Q2 that sets the amplitude limits. Q52 is part of a temperature compensation circuit to maintain the amplitude stability relative to temperature.

A band pass filter L1-L3 and C5-C13 receives an input from the squaring circuit and filters the square wave into a sine wave. The filter output drives the differential amplifier U1, whose two outputs are 180° out of phase. Each output from U1 is buffered by U2 and U3 before driving the low frequency mixer Q5 and Q6.

The four-phase selector (U4-5 from the Frequency Board schematic sheet 1) drives the differential stage Q3 and Q4 on the Output/Power Supply schematic sheet 1. The output of Q3 and Q4 is used to switch the low frequency mixer (Q5 and Q6) between the normal 0° phase and inverted 180° reference signal at the rate of the divided VCO frequency. The mixer products are filtered by a 600 kHz low pass filter leaving the difference signal (the VCO frequency minus reference frequency). The signal is buffered by U5 and Q8. From Q8 the 0 to 500 kHz sine is sent to relays which switch the signal in or out of the output circuits.

If a ramp is programmed, more filtering is required. A RAMP 1 line enables the transistor switch Q7, adding an additional filter capacitor C26

4.5.5 Ramp Waveform

The ramp waveform is a product of the low frequency generator (ref: figure 4-6, the Frequency Board schematic sheets 1 and 2, and the Output/Power Supply schematic sheet 1). A positive ramp is generated by using the portion of the sine wave between the negative and positive peaks. At the positive peak the balanced mixer switches to the inverted sine wave and again the output is from the negative to the positive peak. For a negative ramp, the balanced mixer is enabled between the positive peaks. The "ramp" sine wave is routed through the triangle converter (ref: paragraph 4.7.3) to produce a linear ramp.

As with the other low frequency functions, the mixer requires two inputs: a 1-to-1.5 MHz variable frequency and a 1 MHz reference frequency. The 1 MHz reference input, as for other mixing functions, becomes two 1 MHz sine waves, normal and inverted, applied to the reference input of the balanced mixer (figure 4-6). But, the variable frequency input to the low frequency mixer is modified by the VCO and several sections of the low frequency generator.

First, the VCO frequency is changed to 1 MHz plus one-half the programmed frequency. For example, if the desired output frequency is progammed for a 20 kHz ramp, the variable frequency will be internally programmed to 1.01 MHz (the frequency control logic programs the VCO to 101 MHz and the divide by 100 counter divides the frequency to 1.01 MHz).

Second, the last stage (divide by 2) of the square divide by 100 counter U11 is bypassed to make the divide by 100 counter a divide by 50 counter by enabling gate U19-2,13 with a TTL high.

Third, gate U2-9 (Frequency Board schematic sheet 1, coordinates A7) is enabled via the main

microprocessor's data bus (D0-D7) to place the four-phase selection switch U4-9 in the ramp mode.

The four-phase selection switch switches between the 0° and 180° outputs of the VCO divide by 100 counter. The switching of the four-phase selection switch is controlled by the square divide by 100 counter. Even though the last divide by 2 counter U11-6 is bypassed, it is still operational and its output U11-6 supplies the gate U2-8 with a square wave whose transitions are coincident with the positive and negative peaks of the sine wave from the low frequency mixer output Q8 (Output/Power Supply sheet 1, coordinates B2). The square divide by 100 counter is synchronized by the divide by 100 counter's sync circuits, which function as described in paragraph 4.5.2. The 1 MHz and the variable frequencies are hetrodyned in the low frequency mixer. The resultant, after filtering, is half of a cosine wave from 0° to 180° or its inverse function depending upon the slope of the ramp. The half cosine wave is fed through the triangle converter to create a ramp. The ramp is routed through the waveform selector to the output amplifier.

4.6 TRIGGER CIRCUITS

The 178 can be triggered and gated at frequencies below 500 kHz. This is accomplished by controlling the low frequency generator with internal or external control signals processed by the trigger input and control logic circuit and routed to various sections of the low frequency generator.

Inputs that control the trigger input and control logic circuit are from the front and rear panel BNC's, the instrument's internal sweep generator, GPIB commands and the manual trigger key. Other control lines to the circuit select the trigger slope, the trigger or gate mode and internal or external trigger. The output of the trigger control circuit is digital control lines that control the low frequency generator, the sweep generator, the trigger start/stop circuit and the low-frequency-generator synchronization. Discussion will begin with the trigger theory and then component functions.

4.6.1 Trigger Theory

Figure 4-8 is a simple diagram of the low frequency trigger circuit. The trigger circuit consists of two input frequencies f_1 and f_2, an electronic switch SW1, a programmable delay Θ, and the low frequency mixer.

If the switch SW1 is connected to the variable frequency f_2, f_2 is mixed with the reference f_1 resulting in a difference frequency of $f_2 - f_1$. This difference frequency is what normally would come out of the low frequency mixer in continuous mode. To produce a dc base line associated with trigger function, SW1 switches from f_2 to f_1'. f_1' is the reference from one of the four phase outputs of Q3 and Q4. By mixing f_1 with f_1' a difference frequency of 0Hz or dc is produced. By making SW1 a high speed switch and switching f_1' to f_2 at a rate controlled by a trigger source, a combination of dc, which is $f_1 - f_2'$, plus difference frequency $f_2 - f_1$ will be produced giving trigger control of one, several or many cycles from a dc base line are shown in figure 4-10.

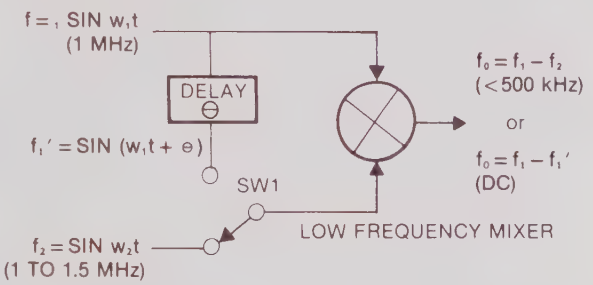


Figure 4-8. Triggered Generator

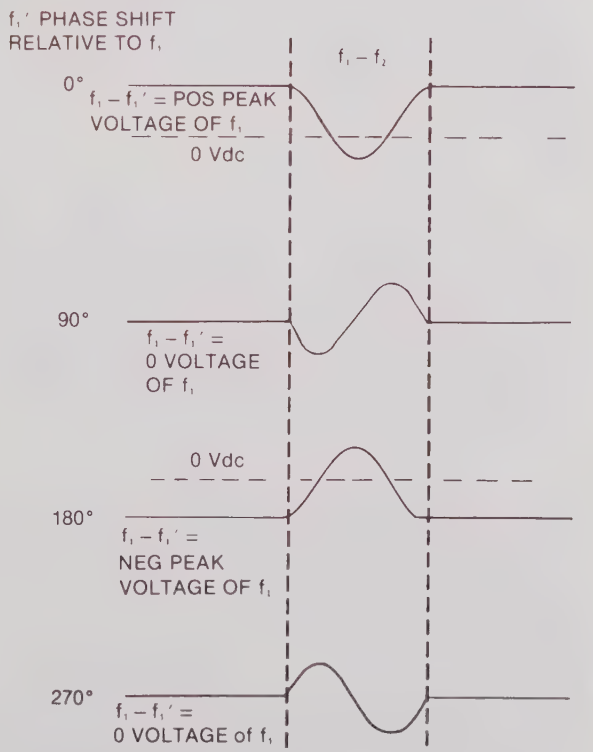


Figure 4-9. Baseline Voltage Controlled By f_1—f_1'

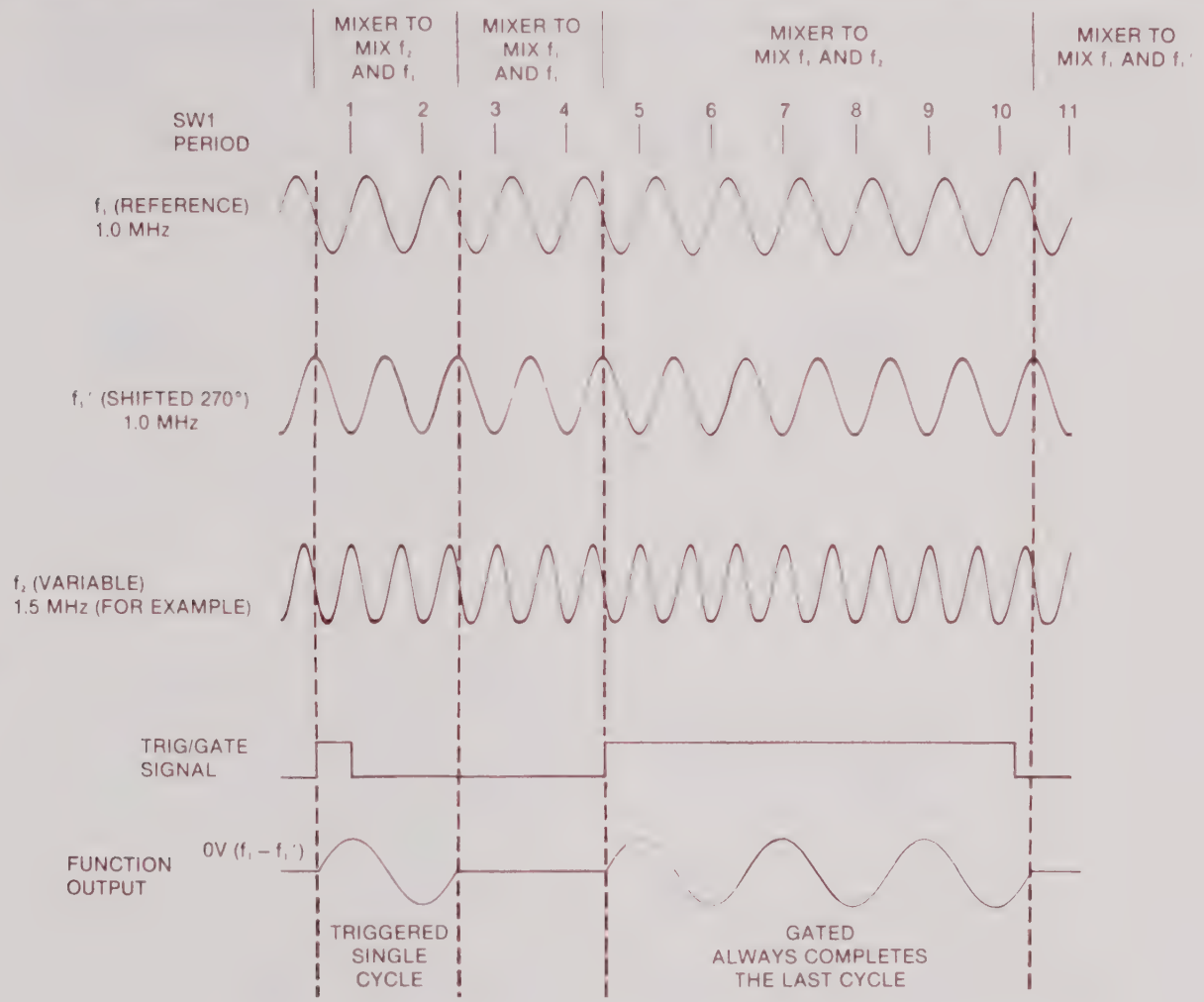

MIXER TO MIX f_2 AND f_1
MIXER TO MIX f_1 AND f_1
MIXER TO MIX f_1 AND f_2
MIXER TO MIX f_1 AND f_1'
SW1 PERIOD
1 2 3 4 5 6 7 8 9 10 11
f_1 (REFERENCE) 1.0 MHz
f_1' (SHIFTED 270°) 1.0 MHz
f_2 (VARIABLE) 1.5 MHz (FOR EXAMPLE)
TRIG/GATE SIGNAL
FUNCTION OUTPUT
0V ($f_1 - f_1'$)
TRIGGERED SINGLE CYCLE
GATED ALWAYS COMPLETES THE LAST CYCLE

Figure 4-10. Trigger/Gate Waveforms

In addition to $f_1 - f_1'$ creating a dc level, changing the phase of f_1' with respect to f_1 will produce three different dc values. For example, as figure 4-9 illustrations, by making f_1' sample f_1 with 0° of phase shift causes only the positive peak to be sampled and hence the dc level $f_1 - f_1'$ is the positive peak value. When the difference of $f_1 - f_1'$ is generated with a 90° phase shift, the dc level $f_1 - f_1'$ will be 0V. A 180° phase shift between f_1 and f_1' will make the dc equal to the negative peak. A 270° phase shift between f_1 and f_1' will give a 0 Vdc level but the waveform phase will be shifted 180°.

4.6.2 Trigger Start/Stop Switch

Refer to the Frequency Board schematic sheet 2 and figure 4-6. The switching takes place before the divide-by-100 counters and is controlled by the trigger control logic. The high speed switch for controlling the mixer inputs consists of U28-6, 7,U29-2, 3, 7, 9, U32-2, 3, 6, 7, U31-4, 5,2 and 3, 6, 7. Refer to figure 4-11 for a simplified picture of the switch. The logic level from the output of the trigger control logic (U14-9, sheet 1, coordinates 3C) is sent with its inversion to U29-7 and U32-7 via U28-6, 7, 9. These logic levels to the data

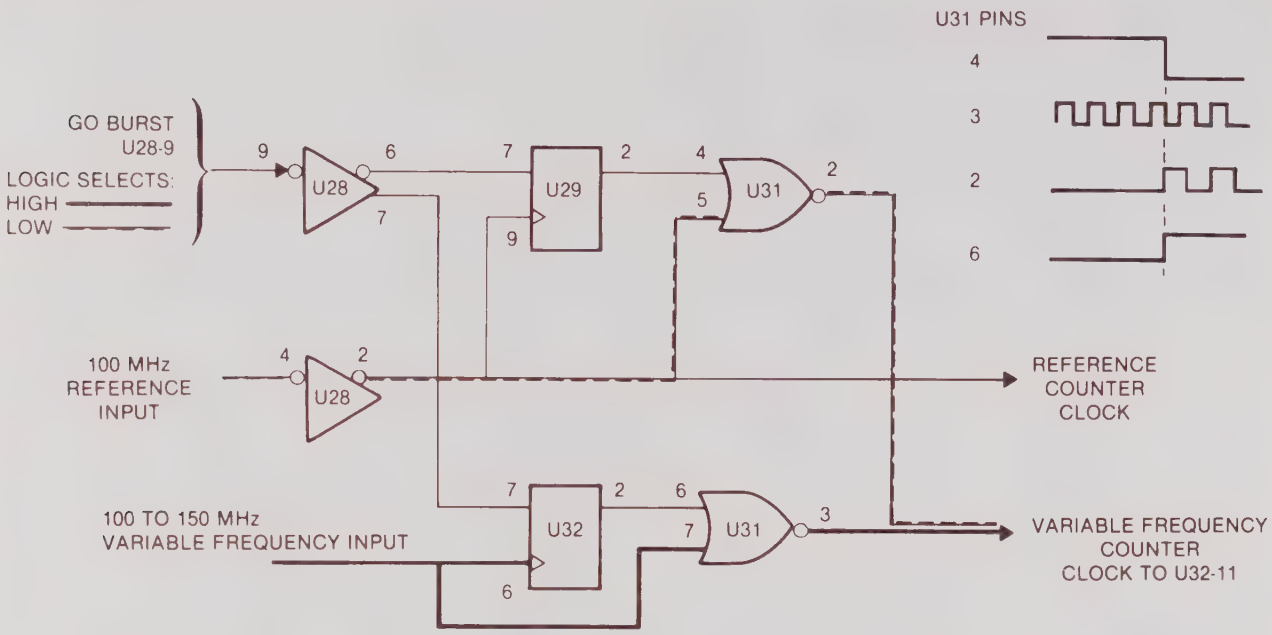


Figure 4-11. Trigger Start/Stop Switch

inputs of U29 and U32 are clocked at a 100 MHz rate to U29-9 and a 100 to 150 MHz VCO rate to U32-6. The resulting input levels to NOR gates U31-4 and U31-6 determine the proper signal to be passed into the VCO divide-by-100 counter.

For example, to produce a difference frequency other than 0Hz, U29-2 must be high and U32-2 must be low. NOR gate U31-2 will not pass the 100 MHz signal to U32-11 but U31-3 will pass the 100 to 150 MHz VCO to U32-11. Thus a waveform wil be produced for the output circuits.

To produce a difference frequency of 0 Hz or a trigger baseline, U29-2 must be low and U32-2 must be high. Thus U31-3 will block the 100 to 150 MHz VCO. The output circuits will be at a dc level determined by the phase that four-phase selector chip (U4-5 on Frequency Board schematic sheet 1, coordinates 7B) is programmed to select.

4.6.3 Trigger Input and Control Logic

The trigger input and control logic receives and processes external and internal trigger signals to control the low frequency generator. Refer to figures 4-6 and 4-12 and Frequency Board schematic sheet 1.

A trigger buffer U9-13 isolates the signal from the front or rear panel BNC and the trigger slope selector U7-2. The slope selector determines whether a positive or negative edge of the external trigger source will enable the low frequency generator. The output from the slope selector is routed through logic gates U8-1 and U9-10. U8-13 and U9-9 also receive signals from microprocessor U42 if a manual trigger from the GPIB is given. The resulting signal output at U9-8 is differentiated by U9, inverted by U15-10, and used to trigger the sweep generator. The other input to U15-9 is from the slope selector U7-8, 9, 10; this line prevents false triggering of the sweep generator when the logic level of U7-12 of the trigger slope is changed.

Internal or external triggering is determined by U16-9. If U16-9 is high, the trigger source will be the internal sweep generator via U16-4, 5. If U16-9 is low triggering will be from the two external sources, GPIB or manual trigger. The GO SWEEP signal comes from U62-9 (sheet 3), coordinates B2. The SWEEP comes from U74-13, coordinates A4. These two signal sources will be discussed in the processor section.

A control line to U8-10 (sheet 1, coordinates C5) decoded from the microprocessor controlled data bus, selects the trigger or gate modes. As with the trigger sweep section, an inhibit command at U15-11 (D3) keeps the low frequency generator from erroneously triggering when the trigger slope is changed.

TEST CONDITION: RESET, PROGRAM MODE (MAIN) TO TRIGGER, APPLY A 500 Hz TTL SIGNAL INTO TRIG IN.

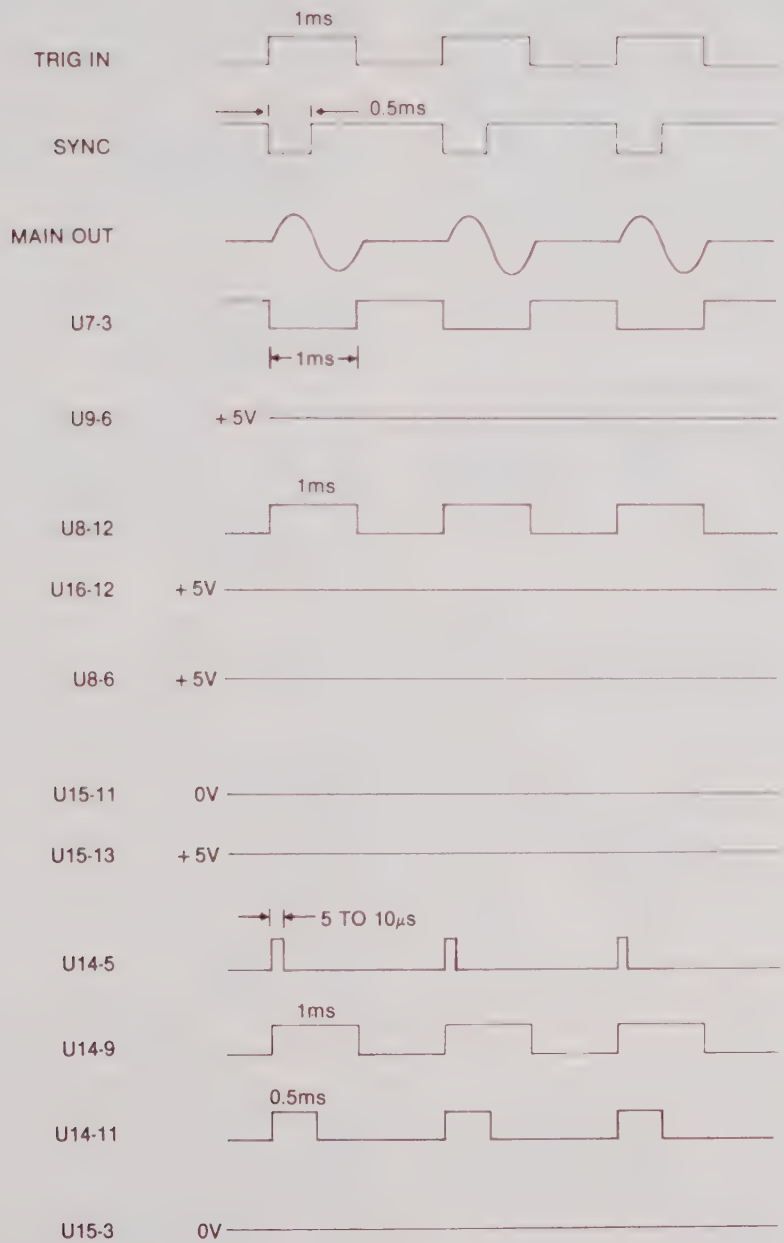


Figure 4-12. Trigger Control Logic Timing (Ref: Frequency Board Schematic Sheet 1)

The flip-flop U14-9 (C3) provides the start/stop control of the low frequency generator. The generator is enabled for a number of periods dependent upon the selected mode: a single cycle for triggered or multiple cycles for gate or burst. This is accomplished by feeding a sync pulse out U6-8 to U43-28, (Frequency Board schematic sheet 3). U43, a burst counter, counts up the number of desired triggered cycles and sends a control signal back to U15-3. This signal controls whether U14 will be set or not. When U14 is set, the low frequency generator is disabled and the sweep generator and counters are reset; thus a dc level is produced. When the set state is removed, the initial change causes the burst counter to start counting and allows the desired waveforms and frequency to appear.

4.7 OUTPUT CIRCUITS

As figure 4-1 demonstrates, the output circuits consist of two waveform shapers, two bandpass switches, and two amplifiers with attenuators. Discussion will begin with the bandpass switches and flow through each function to the output.

4.7.1 Bandpass Switches

There are two microprocessor controlled bandpass switches into the output circuits: the square bandpass switch and the sine bandpass switch.

The square bandpass switch is U36, on Frequency Board schematic sheet 2. The high frequency square enters U36-10 from U37-2 (sheet 7). The low frequency square enters via R46 to U36-7. Output from the switch U36-9 goes to U7-7, Output/Power Supply schematic sheet 2. Here the signal is buffered, shaped, then sent to the sync out differential pair (Q14 and Q15) and the square shaper (Q16, Q17) to U21-13, 14,16. U21 is controlled by the waveform selector.

The sine bandpass switch consists of relay K1 (Output/Power Supply sheet 2) for the high frequency and relay K2 for the low frequency sine. When triangle is selected, K3 goes on and K2 opens.

Amplitude modulation and triangle are the other two waveforms selectable by the 178.

4.7.2 AM Modulator

The AM modulator (figure 4-13, Output/Power Supply schematic sheet 2) is a balanced modulator that produces and output circuit proportional to the product of the AM input signal and the high or low band sine wave. The output from the AM modulator circuit is summed into the preamplifier.

The AM modulator consists of four sections: sine wave input, AM modulation input, balanced modulator and current mirror.

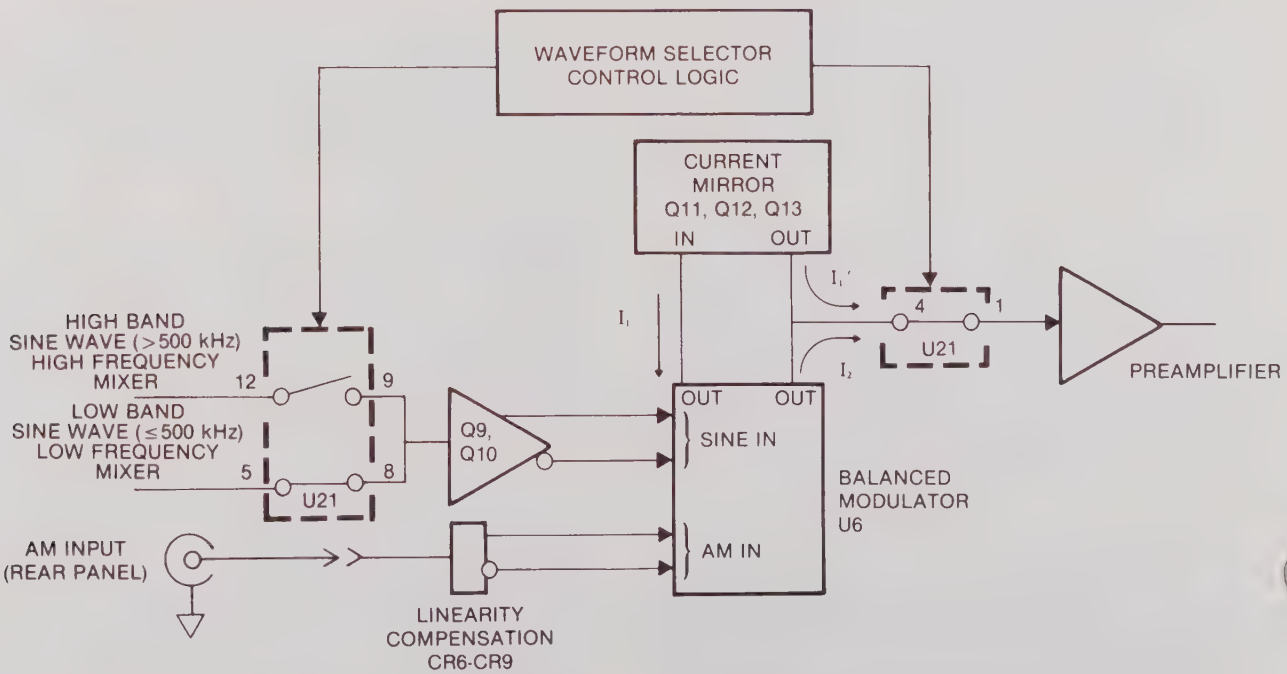


Figure 4-13. AM Modulator

The sine wave input to the balanced modulator is fed through one of two depletion metal oxide semiconductor field effect transistor (DMOS FET) switches U21, coordinates D8. Two control lines from the waveform selector control logic switch the proper DMOS FET switch to select either the high (>500 kHz) or low (≤500 kHz) sine wave band. The sine wave drives an analog amplifier Q9 and Q10 that provides a differential input signal to the balanced modulator.

The AM modulation input, a rear panel BNC, is fed through a diode network CR6-CR9 that is used to compensate for the nonlinear characteristics in the modulator.

The balanced modulator U6 is a single intergrated circuit that produces an output current proportional to the product of the AM modulation signal and the sine wave signal. As figure 4-13 demonstrates, this modulator has differential outputs which drive Q11 of the current mirror (I_1) and half of the preamplifier summing node (I_2).

The current mirror Q11, Q12 and Q13 converts the differential output I_1 of the balanced modulator to a single ended output I_1'. I_1' is equal in magnitude and phase to the input current I_1. The current I_1' from the current mirror and the output current I_2 from the balanced modulator are summed through the DMOS FET switch U21 into the preamplifier.

DMOS FET switch U21 controls the path between the balanced modulator output and the preamplifier. When AM is selected, the FET switch is enabled by a control line from the waveform selector control logic to allow the current to flow from the AM modulator circuit to the summing node of the preamplifier. When any other waveform is selected the DMOS FET switch is disabled, thus opening the path between the modulator and the preamplifier.

4.7.3 Triangle Converter

The triangle converter (Output/Power Supply schematic sheet 2) synthesizes a triangle from the low band sine

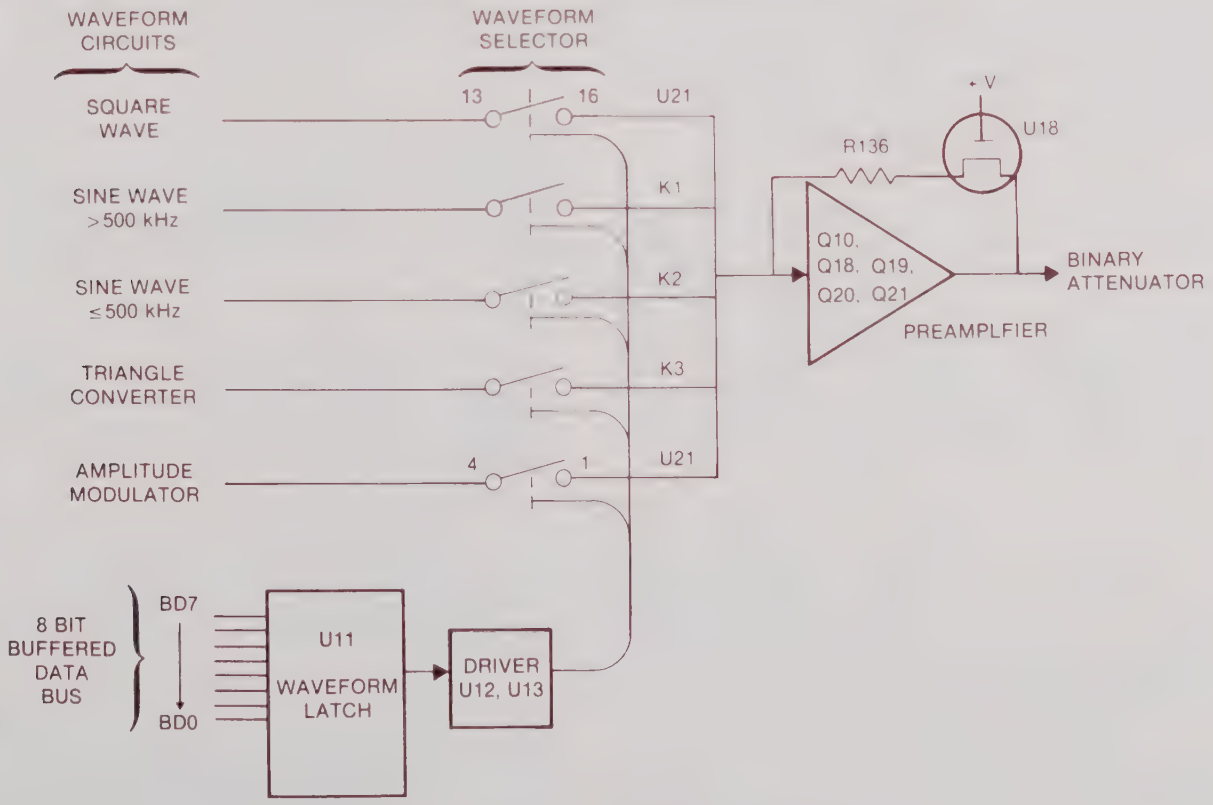


Figure 4-14. Waveform Selector and Preamplifier

wave only. The triangle converter consists of a summing amplifier U8 with a diode network in its feedback path. The input to the triangle converter is a 1.2 Vp-p sine wave from the low frequency generator. The output is a 2.5 Vp-p triangle which is routed through the waveform selector to the preamplifier.

When a ramp is selected, the low frequency generator submits peak-to-peak half sine waves to be converted by the triangle converter to linear ramps.

4.7.4 Waveform Selector

The waveform selector with control logic (figure 4-14 and Output/Power Supply schematic sheet 2), selects one of the six waveforms (square >500 kHz, ≤500 kHz, sine triangle, AM and dc) which will be routed to the preamplifier.

The waveform selector is a combination of DMOS FET's (U21) and relays K1, K2 and K3, which are used as switches as illustrated in figure 4-14. When enabled, the switch presents a low impedance path between the waveform circuit and the preamplifier. Disabled, the switch appears as a high impedance path or open between the waveform circuit and the preamplifier. Each switch is enabled by TTL low and it is disabled by a TTL high. Only one switch at a time can be enabled. If the dc mode is selected, all switches are disabled.

Each switch is controlled by the waveform control logic consisting of U11 with buffer U12 and U13. The control logic data is received from the eight bit buffered data bus and converted to a single control line for each switch by the latch U11. U11 only does this when the WAVE line is enabled. The output from latch U11 drives buffers U12 and U13 before being fed to the waveform selector switches. Table 4-1 is a truth table for the waveform control logic.

4.7.5 Preamplifier

The preamplifier (figure 4-1, and Output/Power Supply schematic sheet 2) sums input currents selected by the waveform selector and supplies a fixed peak-to-peak level to the binary attenuator.

The preamplifier is an inverting amplifier which is composed of a high speed ac amplifier Q18, Q19, Q20 and Q21 and a dc amplifier U10. Feedback for the amplifier is a resistor R136 and a DMOS FET U18 in series; this FET is biased on and compensates for the FET impedance in the binary attenuator. An ac current is summed at the input of the preamplifier and amplified to a fixed level: 3 Vp-p for sine waves square waves and triangles and 1.5 Vp-p for an unmodulated AM, output.

4.7.6 Binary Attenuator

The binary attenuator (figure 4-1 and Output/Power Supply schematic sheet 2) controls the waveform amplitude within each of the four decade ranges. The decade range is determined by the output attenuator.

The binary attenuator block consists of the control logic, the bit selection switches, and the resistor attenuators.

U11 and U14 the control of the attenuator, receive inputs from the microprocessor. Eight output lines from U14 plus two lines from U11 drive level translator U15, U16, and U17. These level translators change a TTL high into a +15V level and a TTL low into a −5V level.

Each of 12 output lines of U15, U16 and U17 is labeled in a binary increment. Whenever any of the lines are activated, the signal is sent through a FET switch and resistor network which will cause an output amplitude equal to 10V times the activated line

Table 4-1. Waveform Control Logic

WAVEFORM	KEY ENTRY	FUNCTION CONTROL LOGIC							BUFFERED DATA U11							
		AMH	AML	AMON	SQUARE	K1	K2	K3	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SINE WAVE >500k	C0	1	1	1	1	0	1	1	X	X	0	0	0	0	0	1
SINE WAVE ≤500k	C0	1	1	1	1	1	0	1	X	X	0	0	0	1	0	0
TRIANGLE	C1	1	1	1	1	1	1	0	X	X	0	0	0	0	1	0
SQUARE WAVE	C2	1	1	1	0	1	1	1	X	X	0	0	1	0	0	0
RAMP	C3	1	1	1	1	1	1	0	X	X	0	0	0	0	1	0
DC	C4	1	1	1	1	1	1	1	X	X	0	0	0	0	0	0
AM (SINE WAVE)> 500k	C5	0	1	1	1	1	1	1	X	X	1	0	0	0	0	0
AM (SINE WAVE) ≤500k	C5	1	0	00	1	1	1	1	X	X	0	1	0	0	0	0

1 = TTL HIGH 0 = TTL LOW X = DON'T CARE

Table 4-2. Examples of Programmed Amplitudes

		BUFFERED DATA (MAIN MICROPROCESSOR)										
		U14								U14	U11	U11
		DB7	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6
		FET SWITCH LINES										
		$\overline{5\ 12}$	5 12	2 56	1 28	64	32	16	08	04	02	01
PROGRAMMED AMPLITUDES (EXAMPLES)	1 00V	1	0	0	0	1	1	0	0	1	0	0
	1 76V	1	0	0	1	0	1	1	0	0	0	0
	2 00V	1	0	0	1	1	0	0	1	0	0	0
	3 00V	1	0	1	0	0	1	0	1	1	0	0
	9 99V	0	1	1	1	1	1	0	0	1	1	1
	10 00V	0	1	1	1	1	1	0	1	0	0	0

1 = TTL HIGH
= + 15V FET SWITCH ON

0 = TTL LOW
= – 5V FET SWITCH OFF

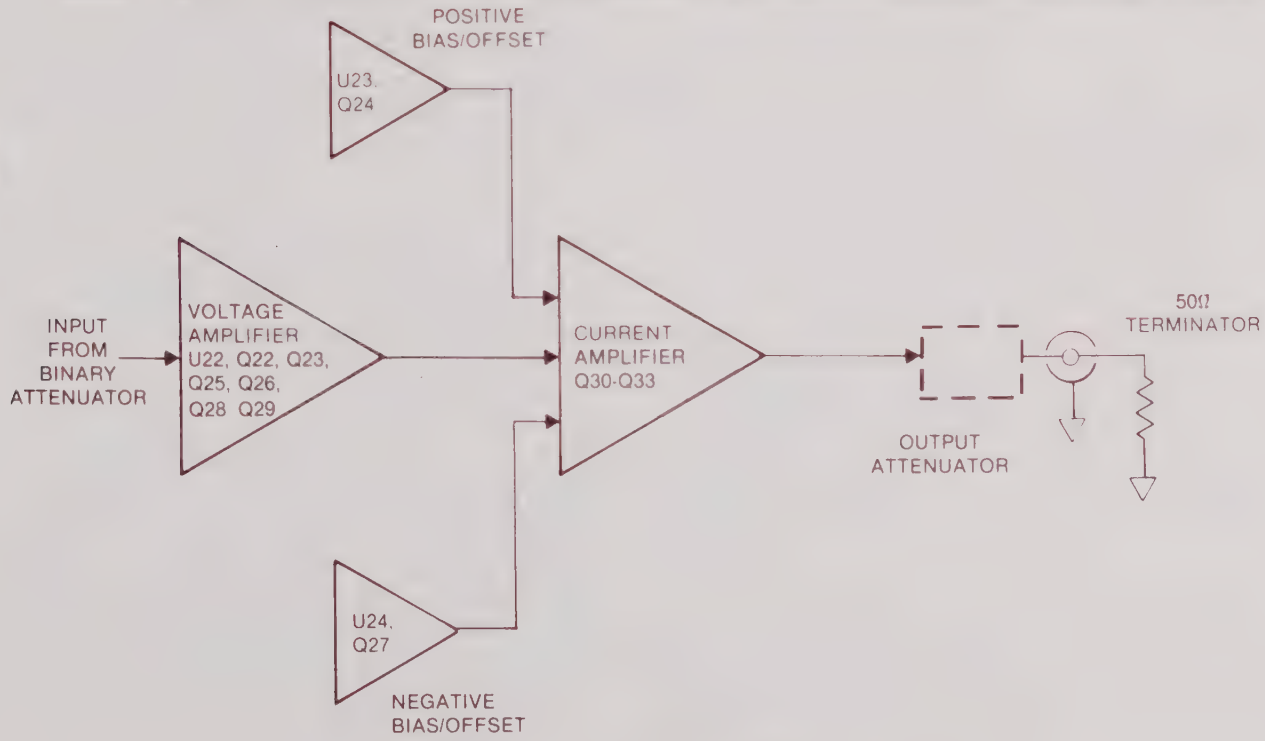


Figure 4-15. Power Amplifier

(assumming the output attenuator is set for 0dB attenuation). Thus if only the .08 line was activated the output would be .8V. See table 4-2 for further examples.

Since the signal flows through the FET's, and each FET has approximately 30Ω's resistance, the FET along with its respective resistor network is made to be part of the preamplifier feedback path.

The $\overline{5.12}$ is only used by itself, while the 5.12 is used in combination with other networks.

Input to the attenuator comes from the preamplifier (TP3) and the output, P.A.SUM, goes to the power amplifier. The resistors connected to each FET constitutes the individual attenuator networks.

4.7.7 Power Amplifier

The power amplifier (figures 4-1 and 4-15 and Output/Power Supply schematic sheet 3) is an operational amplifier with a wide frequency response and low distortion output. The power amplifier receives its input from the binary attenuator and produces an output current, 100 mA peak into 50Ω termination, to the attenuator and, ultimately, the function output BNC's. In addition to amplifying the waveform, the power amplifier is used to offset the dc level of the function output to a maximum offset of ±10V into a 50Ω termination.

The power amplifier consists of three sections: the voltage amplifier, current amplifier and the bias/offset sources. Figure 4-15 shows the interconnections between the three sections and how they relate to their external inputs and outputs.

Basically, the voltage amplifier receives an input current from the binary attenuator, and its output controls the current supplied by the current amplifier to the output load. The bias/offset source provides the bias voltage for the current amplifier.

The following sections describe in greater detail the three sections of the power amplifier.

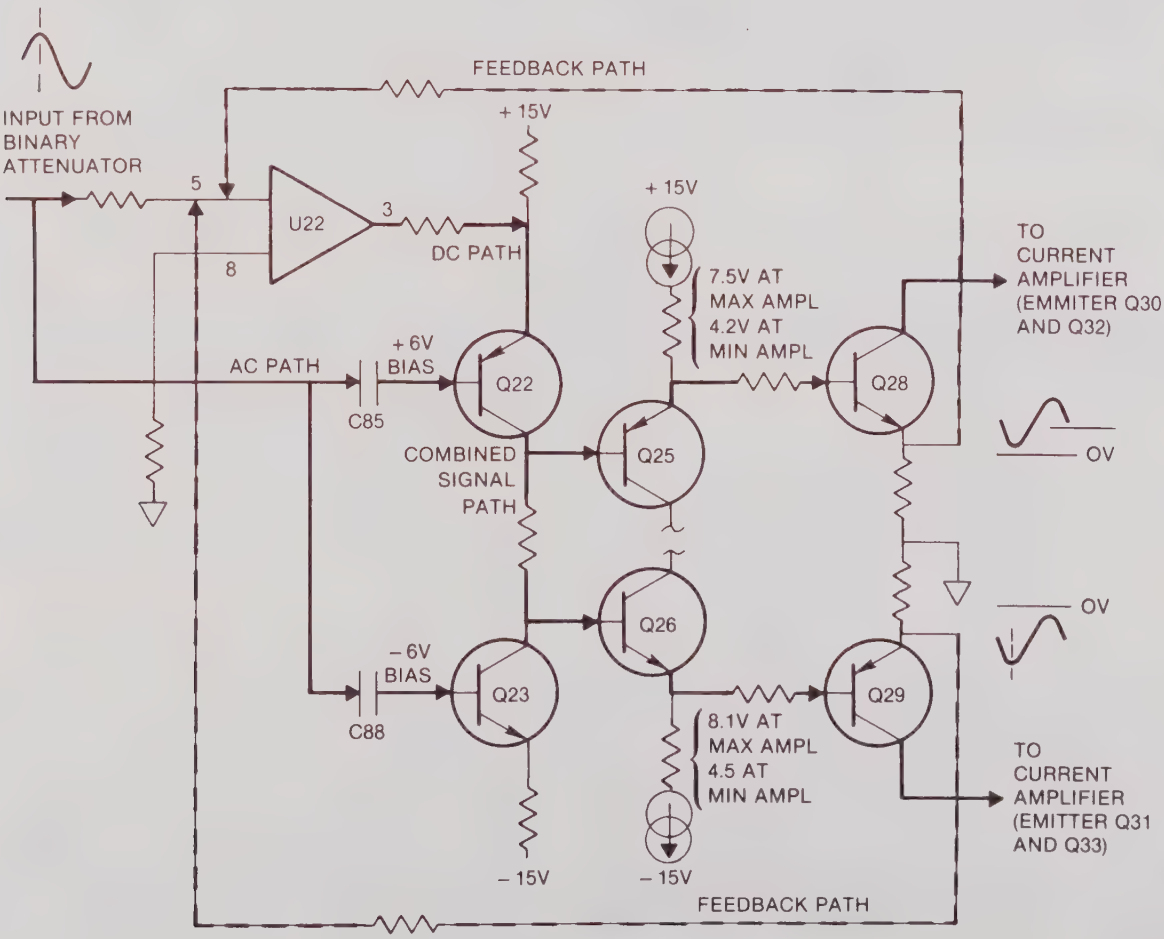


Figure 4-16. Voltage Amplifier

The voltage amplifier consists of U22, Q22, Q23, Q25, Q26, Q28 and Q29. Signal flow through the voltage amplifier is shown in figure 4-16. The voltage amplifier has a dc and ac signal paths; the dc path is through U22 to the emitter of Q22 and the ac path is through C85 and C88 to the bases of Q22 and Q23 respectively. Feedback for the voltage amplifier is taken from the emitters of the output transistors: one feedback path is from the emitter of Q28 and the other path is from the emitter of Q29. The voltage amplifier outputs are the collectors of the transistors Q28 and Q29, which are directly connected to the input of the current amplifer.

The current amplifier (figures 4-15 and 4-17 and Output/Power Supply schematic sheet 3), Q30, Q31, Q32 and Q33 supplies the output current to the output attenuator and, ultimately, to the function output BNC's. There are two inputs to the output attenuator and, ultimately, to the function output BNC's. There are two inputs to the current amplifier: an ac control current from the voltage amplifier and the dc bias/offset voltage which controls the dc offset level at the function output BNC's. Figure 4-17 shows the current flow in the current amplifier for a maximum output signal, 200 mA peak into a 50Ω load.

The bias/offset sources control the bias voltage of the current amplifier and, when controlled by the dc offset circuit, will vary the dc offset level at the function output BNC's. At 0V dc offset, the base of the current amplifier transistors are biased at + and − 12Vdc. U23 and Q24 supply the +12V bias to Q30 and Q32, while U24 and Q27 supply the −12V bias to Q31 and Q33.

To offset the output signal, the dc offset circuit changes the dc levels of the bias/offset sources. For a positive offset, the bias on Q30 and Q32 is decreased causing an increased current flow to the load and the negative bias to Q31 and Q33 is increased causing a decreased current flow. For a negative offset the conditions are reversed: the positive bias on Q30 and Q32 is increased and the negative bias on Q31 and Q33 is decreased.

4.7.8 DC Offset Circuit

The dc offset circuit (figure 4-1, 4-18 and Output/Power Supply schematic sheet 3) controls the level of dc offset present at the function output. The output signal may be offset a maximum of plus or minus 10.00V into a 50Ω termination with a maximum resolution of three digits. The actual maximum offset is dependent upon the programmed amplitude and dc offset; when an internal predetermined limit is exceed, the microprocessor signals the user of a programming error via the front panel display.

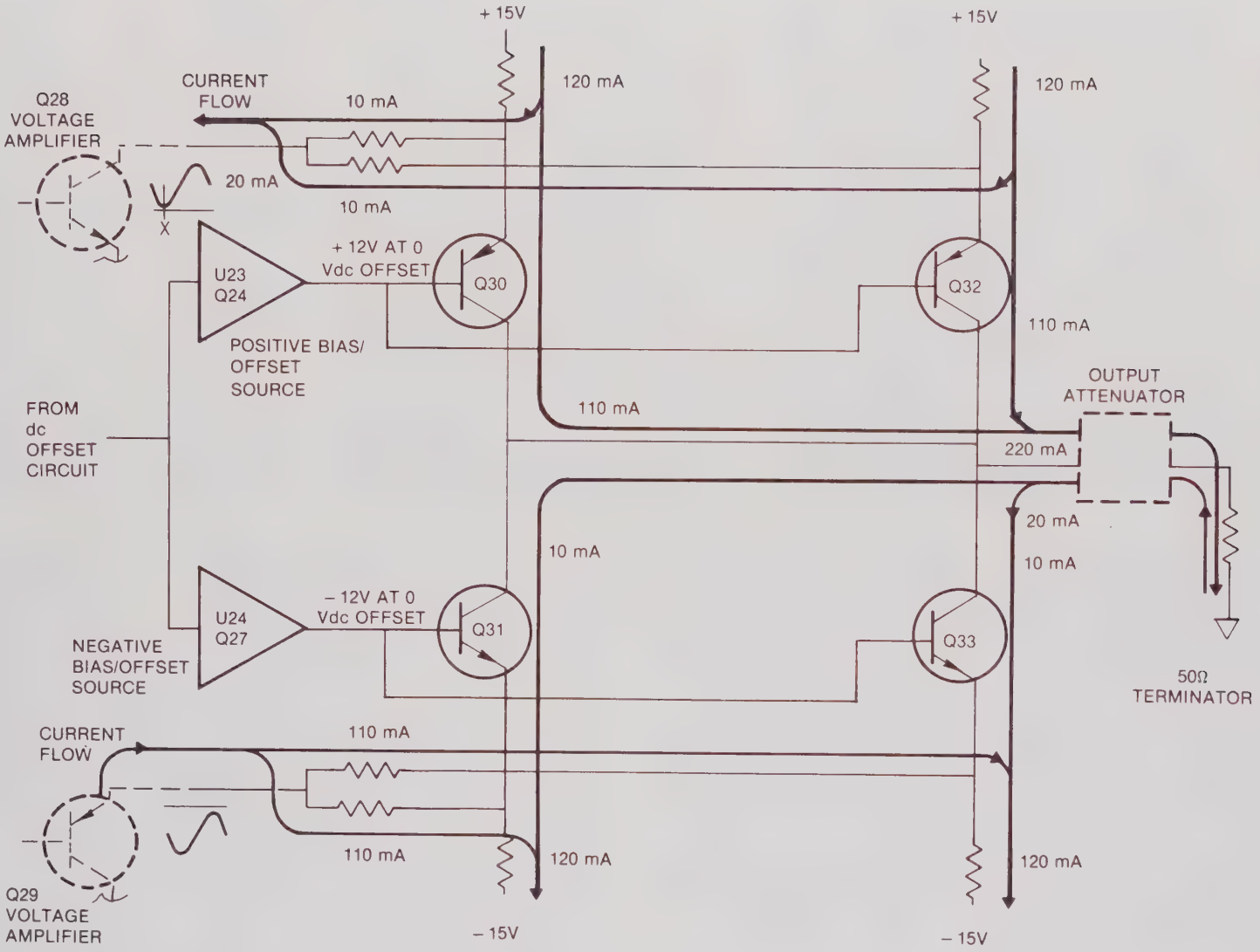
The dc offset circuit operation is best shown by following figure 4-18. The offset latch U25 and U26 receives data of the main microprocessor controlled buffered data bus from the data latch U41 (Frequency Board schematic sheet 3) and transfers the data to the DAC U27 when the latches are enabled by two commands originated at the address decoder U46 (Frequency Board schematic sheet 3); OFST HI enables latch U25 and OFST LO enables latch U26. The DAC U27 converts the 10 bits (3 digits) of digital data from the offset latches into a proportional output current. The operational amplifier U28 sums the current from the DAC to produce an output voltage level proportional to its input current. The maximum output level at U28 pin 6 (TP4) is approximately +7.5V for a programmed offset of 10.00V. The level at TP4 will remain a positive value regardless of whether a positive or negative offset is programmed.

Amplifier U29 and switch U30 determines the polarity of the dc offset level. Switch U30 selects the configuration of the amplifier U29. The polarity control line from the offset latch U25 (BD7, OFST HI); a TTL low selects the positive offset levels and a TTL high selects the negative offset levels. When a positive dc offset is selected, as shown in figure 4-18, the amplifier U29 is configured as a voltage follower which supplies a positive input current to the power amplifier. For a negative dc offset, the conditions of the switch U30 are reversed (U30 pins 3 and 4 are shorted and pins 11 and 12 are open) connecting the amplifier U29 as a unity gain inverting amplifier which supplies a negative current input to the power amplifier.

The current from the dc offset circuit is applied to two scaling resistors R177 and R187. R177 is the input resistor for the positive dc offset source U23, and R187 is the input resistor for the negative dc offset source U24.

4.7.9 Output Attenuator

The output attenuator reduces the current supplied by the power amplifier in 20 dB steps. Three sections of resistor attenuators are used to attenuate 20 dB through 60 dB, and a single line is used to bypass the attenuator network for 0 dB (figure 4-19).



NOTE: Current is an instantaneous positive peak current relative to the positive peak of the power amplifier input signal

Figure 4-17. Current Amplifier and Bias/Offset Amplifier

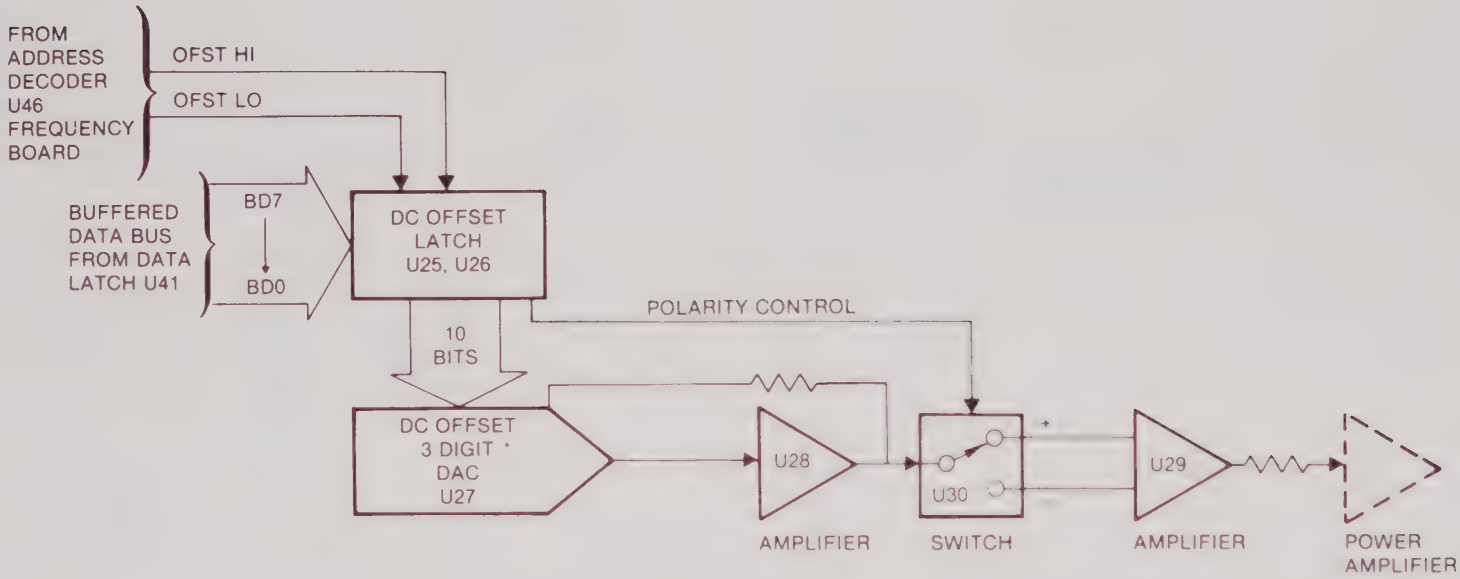


Figure 4-18. DC Offset Circuit

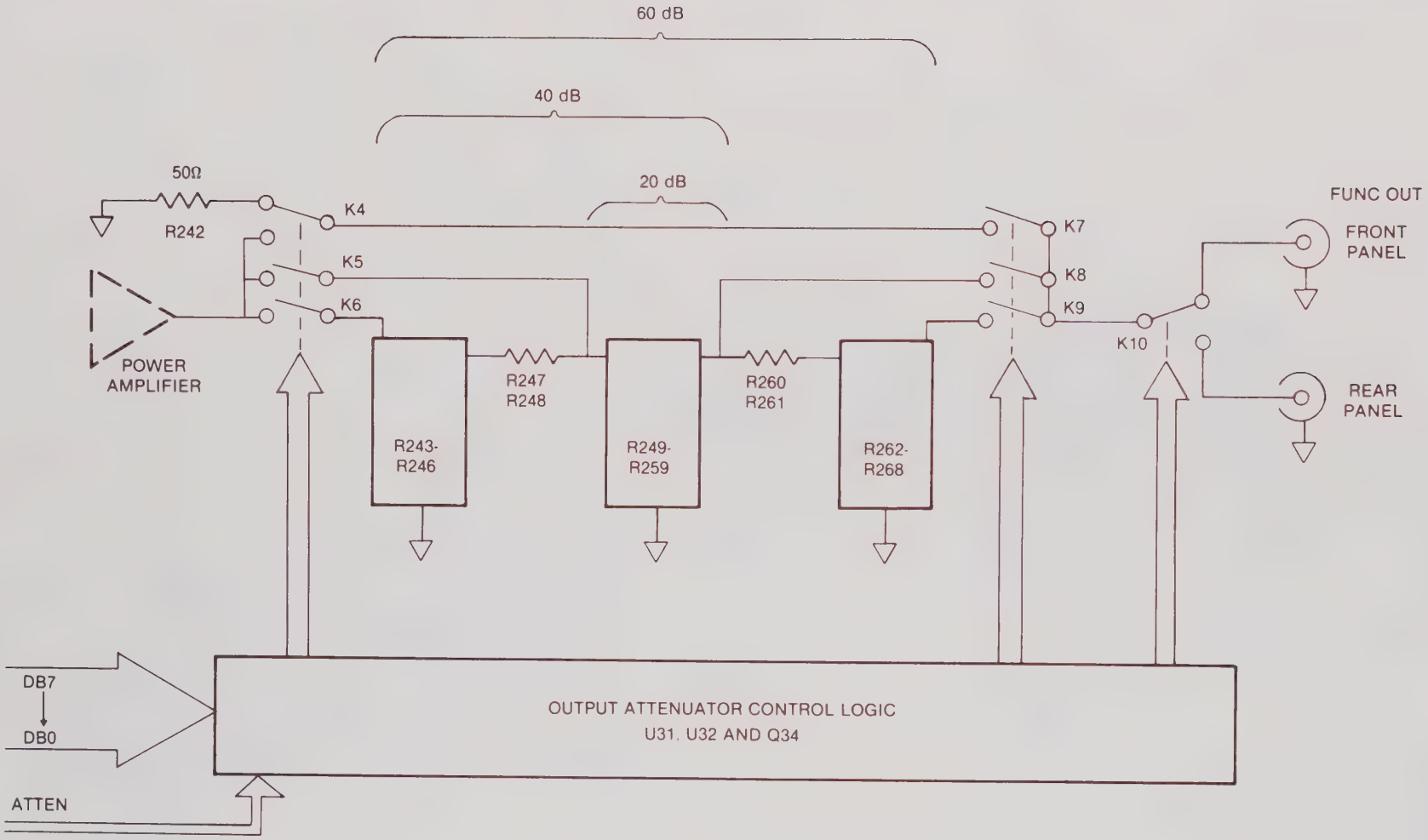


Figure 4-19. Output Attenuator

Table 4-3. Output Attenuator Control Logic

1 = TTL HIGH
= RELAY ON

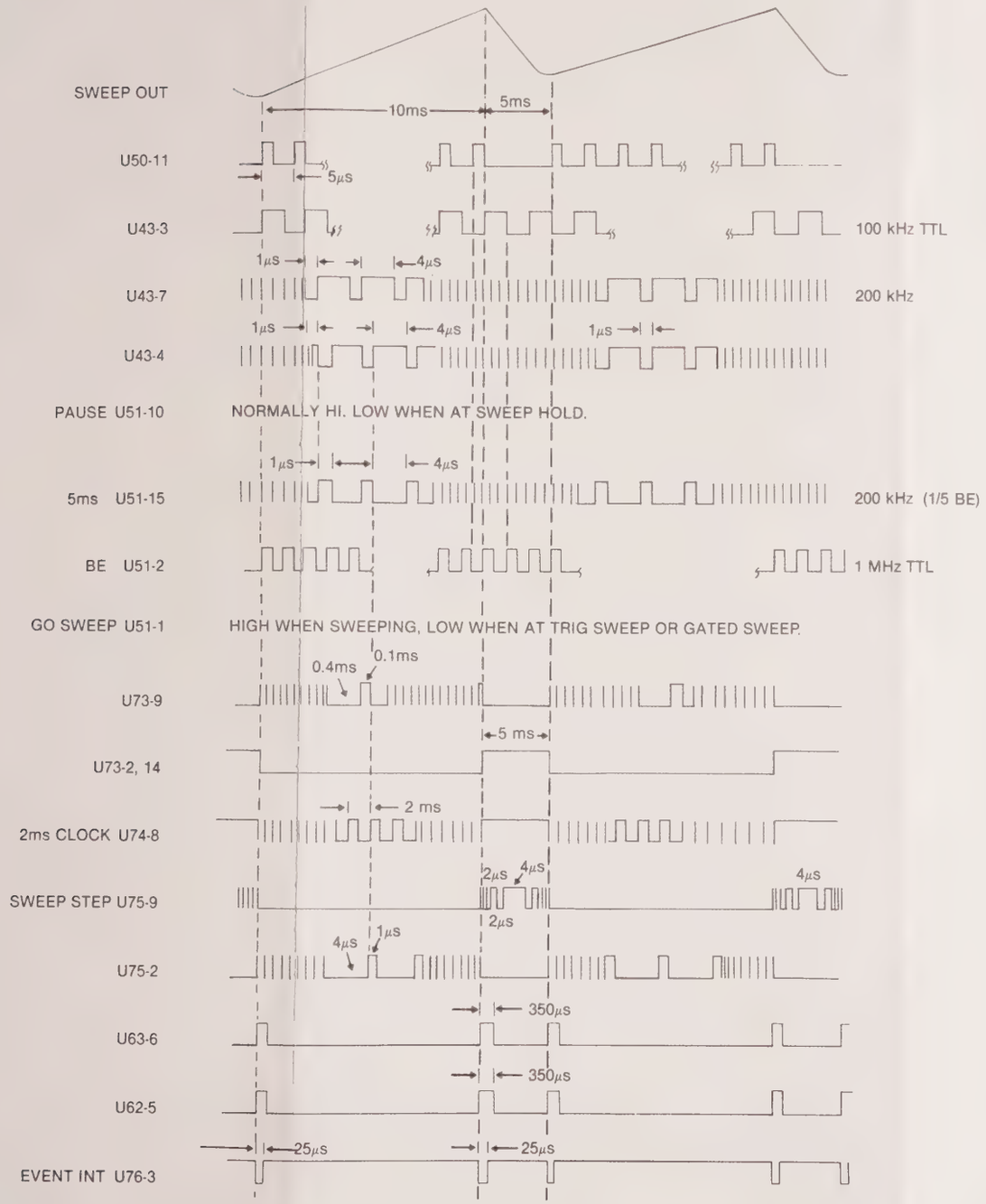
0 = TTL LOW
= RELAY OFF

X = DON'T CARE

					BUFFERED DATA BUS							
					BD6	BD5	BD4	BD3	BD2	BD1	BD0	
					U31 PIN NUMBER							
					16	2	12	15	5	6	9	
OUTPUT ATTENUATOR	OUTPUT	INTERNAL LOAD	FUNCTION OUTPUT BNC	KEY ENTRY	RELAYS							AMPLITUDE RANGE (Vp-p AT 0Vdc OFFSET)
					K10	K4	K5	K6	K7	K8	K9	
0 dB	ON	OUT	X	E0P1	X	1	0	0	1	0	0	20.00 - 10.02
0 dB	ON	IN	X	E0P1	X	1	0	0	1	0	1	10.00 - 1.01
– 20 dB	ON	IN	X	E-1P1	X	0	1	0	0	1	0	1.000 - 0.101
– 40 dB	ON	IN	X	E-2P1	X	0	0	1	0	1	0	0.100 - 0.0101
– 60 dB	ON	IN	X	E-3P1	X	0	0	1	0	0	1	0.0100 - 0.001
X	OFF	IN	X	P2	X	0	0	1	1	0	0	X
X	OFF	OUT	X	P0	X	0	0	1	0	0	0	X
X	X	X	FRONT	XP0	0	X	X	X	X	X	X	X
X	X	X	REAR	XP1	1	X	X	X	X	X	X	X

CONTINUOUS SWEEP LINEAR

NOTE: 1. SWEEP MODE = 1 (LINEAR SWEEP); SWEEP TIME = 10ms.
NOTE: 2. TIMING RELATED TO SWEEP-OUT SIGNAL ONLY UNLESS OTHERWISE STATED.



CONTINUOUS SWEEP LOG

NOTE: 1. SWEEP MODE = 4 (LOGARITHMIC SWEEP).
NOTE: 2. SWEEP TIME = 10 ms.

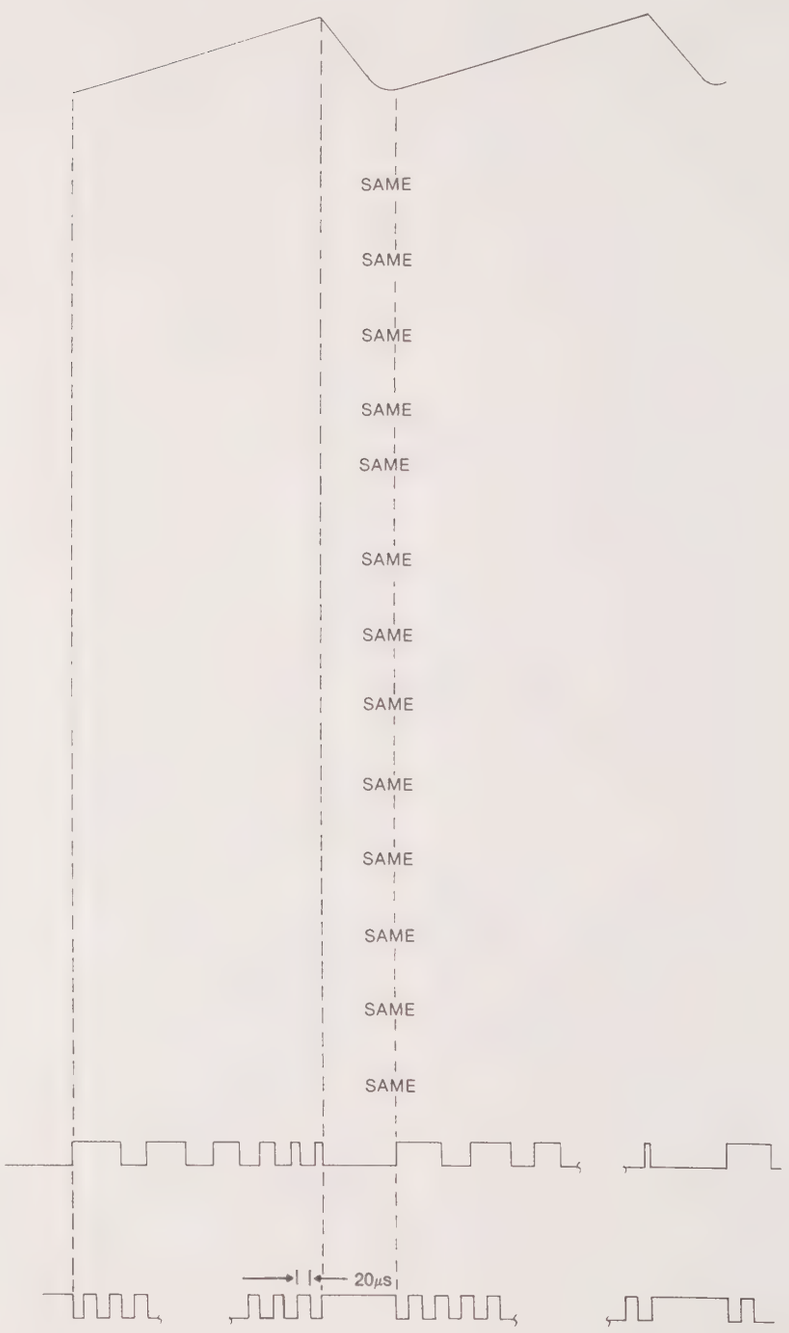


Figure 4-20. Sweep Ramp Generator Timing

The proper attenuator range is selected by the microprocessor. The microprocessor checks the programmed amplitude and dc offset before selecting the proper attenuation range. The microprocessor then sends 8 lines of data (BD0 through BD7) into latch U31. U31 will only transfer the data to its output if the ATTEN line into the chip goes high. From U31's output the respective relay signals are buffered through six buffers (U32) and transistor Q34. The six buffers drive relays K4-K9 for selection of the correct attenuator network. Transistor Q34 causes relay K10 to select front or rear output BNC's. Table 4-3 gives the state conditions required for each attenuator condition.

In addition to controlling the output attenuation, the output attenuator control logic controls several other functions. First, if 0 dB and internal 50Ω termination are programmed; (E0, A1.01 to 10.00), relays K4,K7 and K9 are activated; K4 and K7 bypass the attenuator while K9 will connect the output attenuator (used as a 50Ω termination) across the function output. Second, if the the output is turned off with an infinite source impedance at the function output (P0, A>10.00), relays K7, K8 and K9 are deactivated and relay K6 is activated to load the power amplifier with a 50Ω termination. Third, when the output is turned off with a 50Ω source impedance at the function output (P2) relay K7 and K6 are activated; relay K7 connects a 50Ω resistor R242 across the function output BNC and relay K6 connects the output attenuator, used as a 50Ω load, to the power amplifier output. Fourth, if the output is turned off with an infinite source impedance at the function output BNC, relays K9, K8 and K7 are deactivated, opening the path to the function output BNC. Also, K6 is activated to connect the output attenuator, used as a 50Ω load, to the power amplifier output.

4.7.10 Sweep Ramp Generator

The sweep ramp generator (ref: figure 4-1, and Frequency Board schematic sheets 2 and 3) provides a linear ramp that is proportional to the sweep frequency (ref: paragraph 3.9.4).

The sweep is produced by the ramp generator U17, Q3, Q4, Q5 and Q6 from an input from the programmable counter U43, U48, U49 and U50.

The ramp generator receives a series of 2000 pulses (RAMP STEP) that are controlled by the programmable counter U43. U43 will always supply 2000 pulses which are equivalent the sweep time. As the sweep time varies the frequency of the step pulses change. The ramp step pulses from U50-3 (ref: Frequency Board schematic sheet 3) are applied to the base of Q5 then through Q6 into the integrator U17. Each pulse will cause the sweep output U17-6 to increase by ≈2.5 mV until the output reaches ≈ + 5V. A reset command (RST SW) at Q3 will turn on Q4 or reset the ramp to zero. A timing diagram for the ramp generator circuit is shown in figure 4-20.

4.8 DIGITAL CONTROL

The digital control section (figure 4-1) includes the input/output microprocessor, GPIB interface and keyboard/display interface; these sections control the data in to and out of the instrument. In addition, it includes the main microprocessor and the frequency control logic (digital sweep generator), which control the high frequency generator, low frequency generator and output sections.

Each portion of the digital control section is described in the following sections.

4.8.1 Front Panel

The front panel assembly contains the circuits that receive and process the input parameters, parameter values and actions which are entered from either the keyboard or the General Purpose Interface Bus (GPIB). Also, the front panel contains the display of 178's status.

The front panel (ref: figure 4-1, 4-21 and Display/Logic schematic sheets 1,2 and 3) consists of the keyboard, display, General Purpose Interface Bus (GPIB), input/output (I/O) microprocessor and the microprocessor support circuitry. In addition, the front panel assembly contains four BNCs: Ext Trig In, Sweep Out, Sync Out and Function Out.

The front panel circuits are isolated from the circuit common. Therefore, data output from the front panel to the main microprocessor circuits is optically isolated serial data.

The front panel assembly is connected electrically to the 178 by two ribbon cables and four coaxial cables. One ribbon cable J30 connects the display and keyboard to the frequency board at J15. A second ribbon cable J29 connects the GPIB assembly to the rear panel J19 and J18. Four coaxial cables connect the front panel's BNCs — Ext Trig In (J36), Sweep Out (J35), Sync Out (J34) and Function Out (J33) — to the frequency or the output/power supply boards.

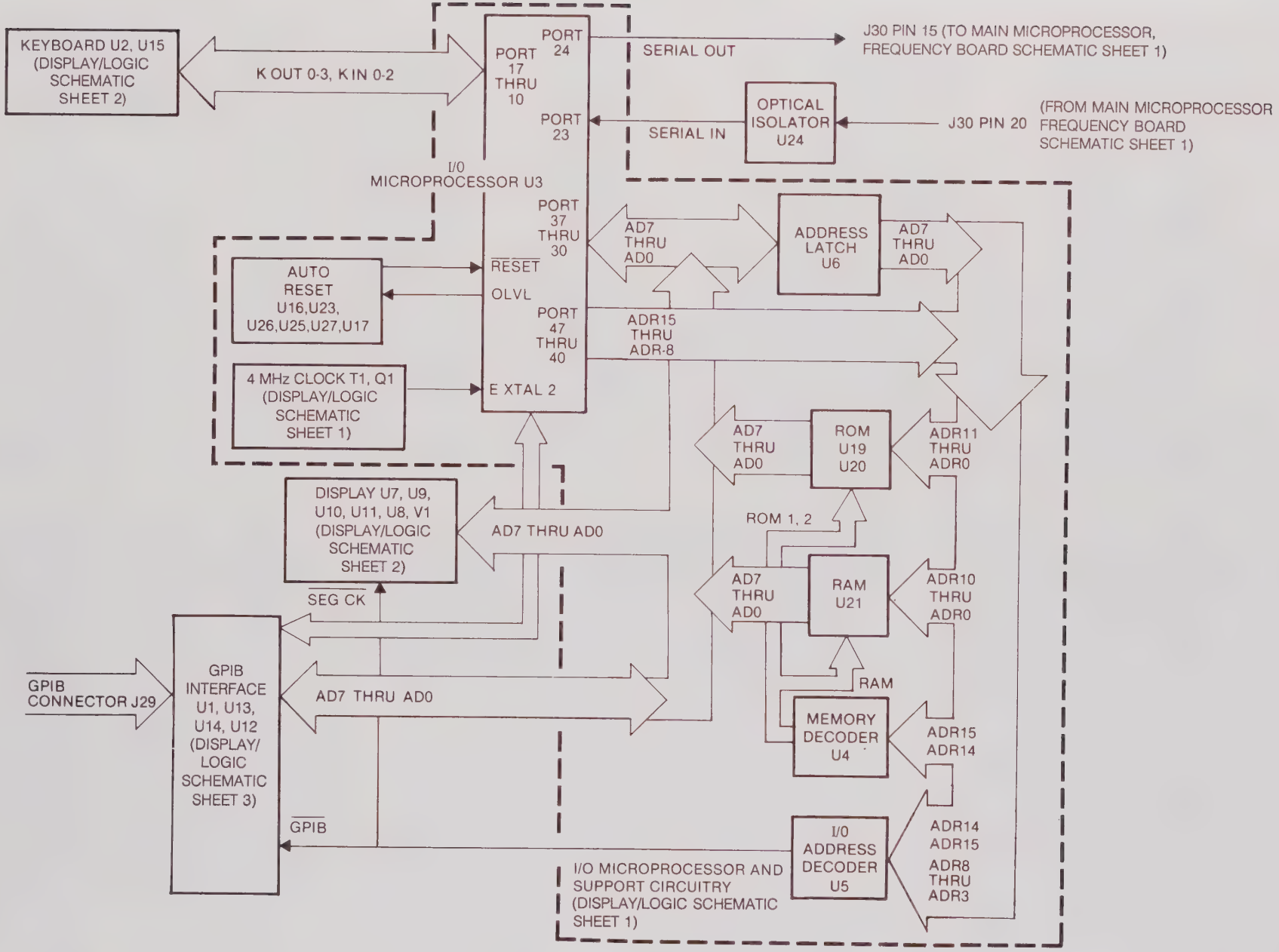


Figure 4-21. Front Panel Circuits

The following sections describe the I/O microprocessor, its support circuits, keyboard, display and GPIB interface.

4.8.1.1 Input/Output Microprocessor and Support Circuits

The input/output microprocessor U3 (ref: Display/Logic schematic sheet 1) acts as the input/output processing unit. It receives input information from the keyboard and GPIB. It processes the information and sends it to the main microprocessor via an optically isolated serial bus. Also, the I/O microprocessor processes output information that is sent to the output ports (GPIB or display). The processing of this information is directed by the software. Software directs the processor to address subsystems and issue commands and data which directs the 178 to output the desired signal.

Software refers to a sequence of commands executed by the I/O microprocessor. This sequence of instructions stored in Read Only Memory (ROM) commands the microprocessor to perform according to the 178 specifications. The microprocessor is powerless without a program to run; therefore, the software is one of the most vital elements of the digital section. All information transfer takes place under the control or supervision of the software. Programs are composed of machine language instructions, messages and tables that provide sequencing information. This data stored in the ROM is programmed into the ROM at the time of manufacture.

The I/O microprocessor support circuits consist of the auto reset circuit U16, U23, U26, U25 and U27, the 4 MHz clock T1, Q1, the address latch U6, the memory decoder U4, the I/O decoder U5, and the memories U19, U20 and U21.

This block receives three inputs. One input is from the keyboard, which the I/O microprocessor controls. The second input is data from the GPIB interface. The third input is the serial data from the main microprocessor.

Auto Reset The auto reset circuit initializes the reset sequence of the I/O microprocessor at power-on or after a power transient interrupt. The reset sequence will reset the instrument to the initial power up conditions (ref: table 2-3, step 3).

The auto reset circuit consists of an oscillator U16 pins 5, 6 and 7, a counter U23 and the control logic U25, U26, U27 and U17.

The oscillator U16 pins 5, 6, and 7 produces a 32 kHz pulse. The pulse is used as the clock input to the counter U23.

The counter determines whether or not the I/O microprocessor will be reset. The counter receives two inputs: the 32 kHz clock from the oscillator and a reset pulse originated by the I/O microprocessor or the counter itself.

At power on, outputs (OLVL, XCLK) from the I/O microprocessor are held high for approximately 100 ms. During the 100 ms period, the counter is clocked by the 32 kHz clock. After 64 ms the counter's output U23 pin 1 goes high. This transistion is routed through U17 pin 4, U25 pin 3 and U17 pin 8 to the I/O microprocessor $\overline{\text{RESET}}$ line U3 pin 6. When $\overline{\text{RESET}}$ goes low the microprocessor begins its power-up initialization process. The power-up initialization processes is controlled by the software contained in Read Only Memory (ROM).

If the initialization process is successful the 178 will be in its initial power-up settings. In addition, the I/O microprocessor begins to send out OLVL pulses from U3 pin 9 at approximately a 1 kHz rate. These OLVL pulses will continually reset the counter every 1 ms. Thus, the counters' output, U23 pin 1, will always remain at a TTL low

If the I/O microprocessor fails to send a OLVL pulse for a period greater than 64 ms, the auto reset circuit will attempt to reset the I/O microprocessor. It will keep doing this until the power is removed or the microprocessor begins sending OLVL pulses.

When reset, all data stored in Random Access Memory (RAM) will be erased except the data stored in RAM with battery back up.

4 MHz Clock The I/O microprocessor is clocked at a 4 MHz rate. The 4 MHz clock is applied to the EXTAL 2 input, U3 pin 3, of the I/O microprocessor through the isolation transformer T1 and the buffer amplifier Q1.

The 4 MHz clock is generated on the frequency board (see schematic sheet 2, coordinates C1). Here the 4 MHz clock is routed from U118 pin 2 through an inverter U59 pin 12 to J15 (schematic sheet 3, coordinates A8) pin 1. On the frequency board J15 pin 1 connects through a cable to the display and keyboard assembly (Displaly/Logic schematic sheet 1) J30 pin 1, which connects to the transformer T1.

Address Latch The address latch U6 (ref: figure 4-21 and Display/Logic schematic sheet 1, coordinates D4) is used to select the lower address bits (ADR0-7).

The address latch is a transparent latch with 8 input lines (AD 0-7) from the I/O microprocessor U3. The address latch is clocked by the AS clock line from the I/O microprocessor U3 pin 39. On the positive going transition of the AS clock, data at the address latch inputs U6 pins 3, 4, 7, 8, 13, 14, 17 and 18 are transferred to the address latch outputs U6 pins 2, 5, 6, 9, 12, 15, 16 and 19.

Memories The I/O microprocessor circuit (Display/Logic schematic sheet 1) consists of two types of memories: Read Only Memories (ROM) for permanent storage of data, and Random Access Memories (RAM) for temporary storage of data.

When a specific ROM is enabled it presents its data on the Address/Data bus (AD0 through AD7). The ROM enabling commands are generated by the Memory Decoder U4.

The Random Access Memory (RAM) is used for temporary storage of data. The RAM's store the first five stored settings, the non-executed generator settings, and the display information.

Memory Decoder The memory decoder U4 (ref: Display/Logic schematic sheet 1, coordinates A4) enables either one of two Read Only Memories (ROM) U19 or U20, or Random Access Memory (RAM) U21 as directed by instructions from the I/O microprocessor U3. The memory decoder is itself a ROM and it is programmed to supply specific digital outputs (ROM1/, ROM2/ and RAM/) for specific address bytes (ADR 14-15 and BE).

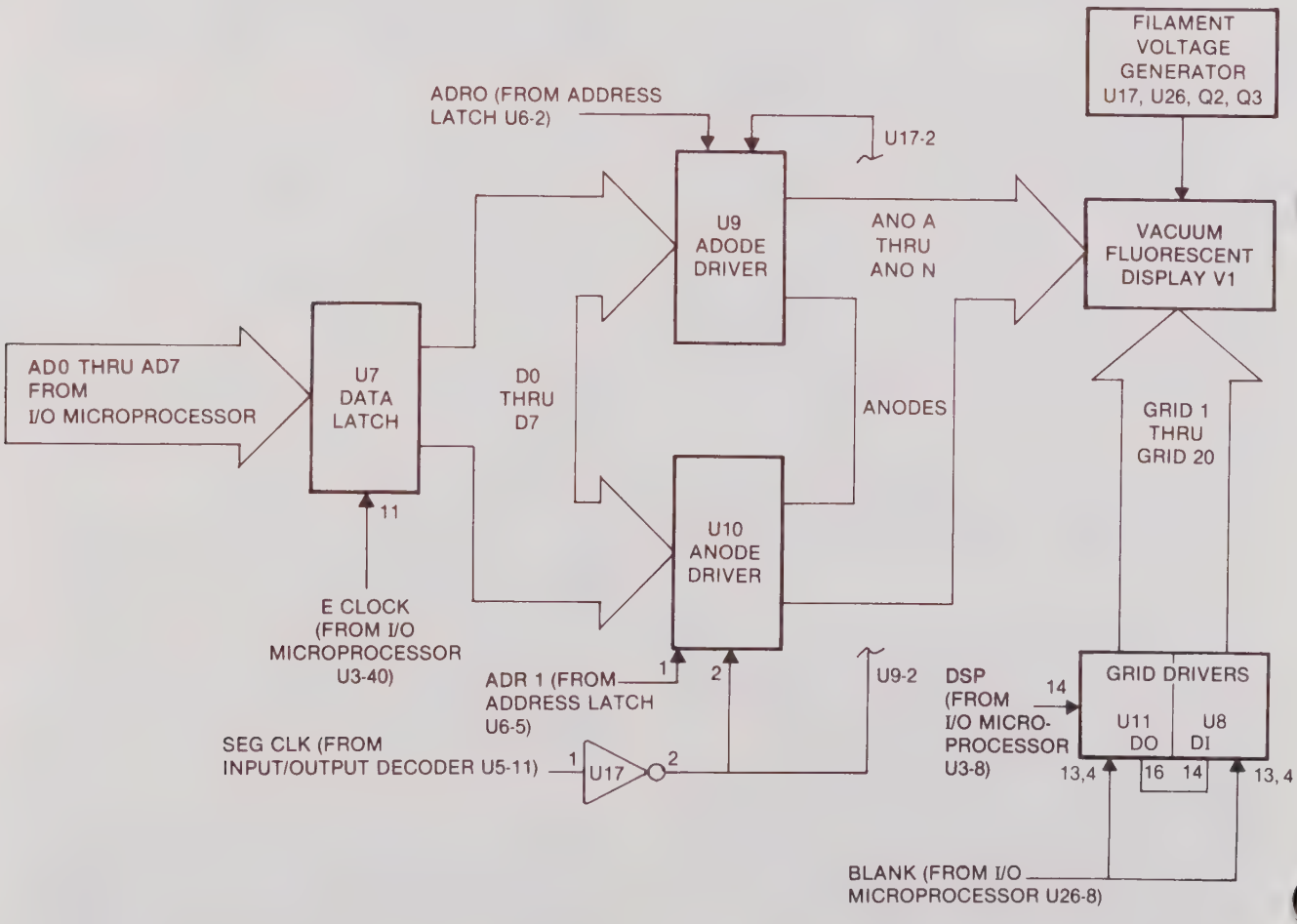


Figure 4-22. Display

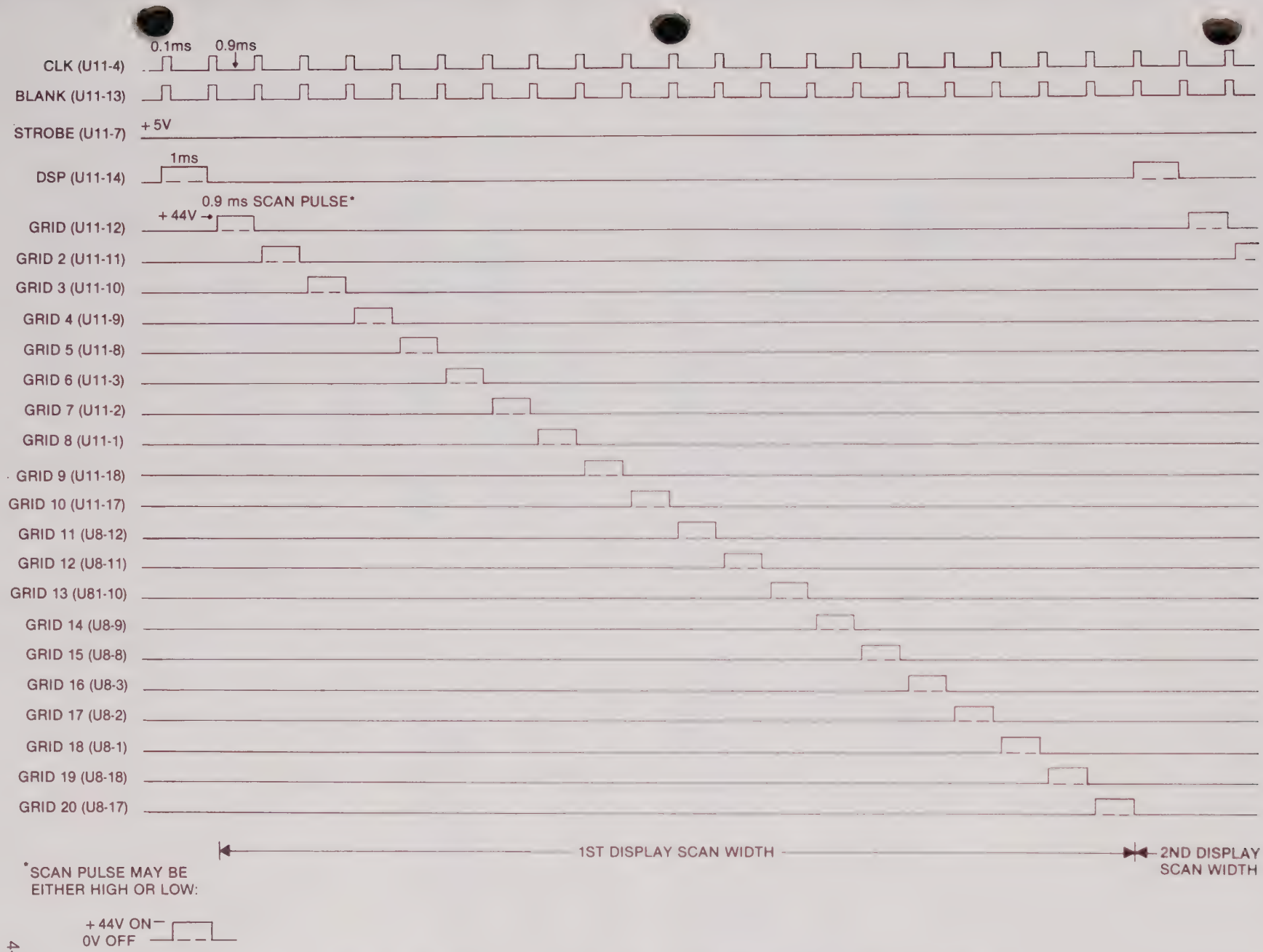
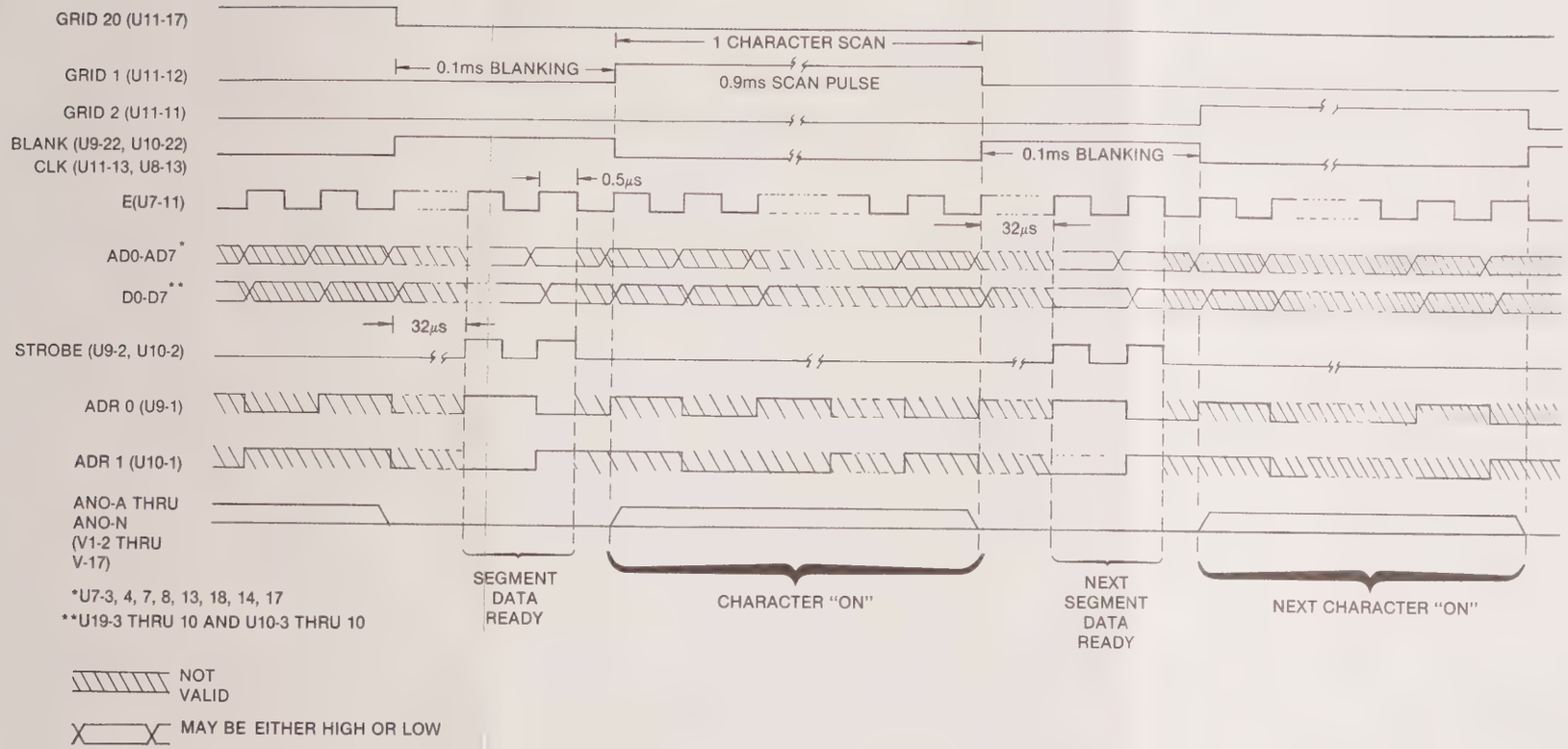
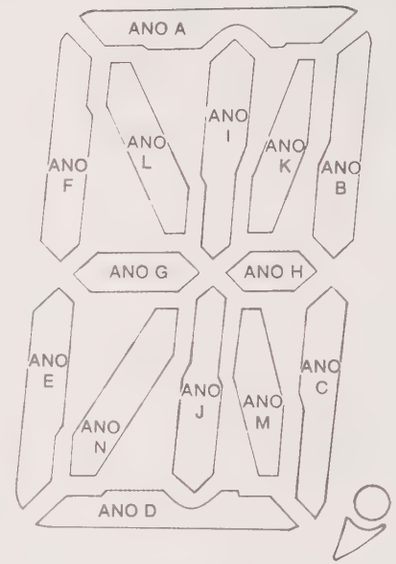


Figure 4-23. Display Logic (Scan Timing) (Ref: Display/Logic Schematic Sheet 1)





DISPLAY SEGMENT DRIVEN (ANODE)	PIN NO.
A	10
B	11
C	6
D	2
E	15
F	12
G	13
H	14
I	9
J	3
K	8
L	7
M	4
N	5
0	17
DP	16

VACUUM FLUORESCENT DISPLAY
(DISPLAY/LOGIC SCHEMATIC SHEET 2, COORDINATES C1)

Figure 4-24. Display Logic (Anode Display Timing)

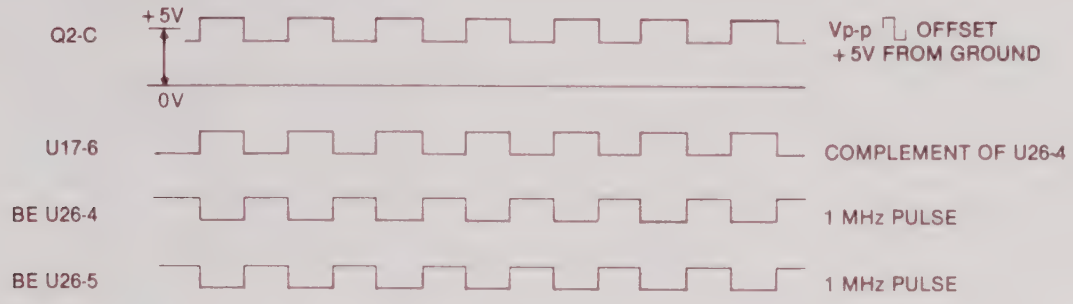


Figure 4-25. Filament Voltage Generator Circuit Timing (Ref: Display/Logic Schematic Sheet 2)

Input/Output The input/output (I/O) address decoder U5 (Display/Logic schematic sheet 1, coordinates A4) enables the GPIB interface processor U1 and anode display drivers U9 and U10, as directed by instructions from the I/O microprocessor. The I/O address decoder is itself a Read Only Memory (ROM) and it is programmed to supply specific digital outputs (GPIB/ and SEG CLK/ for specific address locations (ADR 3-8, ADR 14-15, R/W and E).

4.8.1.2 Display

The front panel display shows the 178's programmed parameters, parameter values and actions.

The display block (ref: figure 4-1, 4-21, 4-22 and Display/Logic schematic sheet 2) consists of the fluorescent display V1, anode drivers U9, U10 and U7, grid drivers U8 and U11, and the filament voltage generator U26, U17, Q2, Q3, and T2.

The fluorescent display V1 is a 20 character display. Each of the 20 characters or grids contains 16 segments or anodes. The fluorescent display is driven by the grid driver U8 and U11, and the anode driver U9 and U10.

The display circuit receives input data and commands from the input/output microprocessor U3. This data is converted into the information required to turn on the grids and anodes necessary to create the desired characters.

Each grid is sequenced on or off as needed. If a grid is turned on, the appropriate anodes must also be selected to light the desired character.

The following describes the data flow sequence required for turning on the grids (ref: figure 4-22). First, the DSP line U11 pin 14 from the I/O microprocessor will be either high or low. A high defines a grid as being turned on and a low defines the grid as being off or a blank. Each BLANK clock shifts the DSP data into the lower order (GRIDS 1-10) grid driver U11. Then the overflow from U11 (DO) is shifted in U8 (DI) which is shifted through U8. U8 contains the upper order grids (GRIDS 11-20). Grid display timing is shown in figure 4-23.

Synchronous with each grid pulse is the data required to turn on the proper anodes, thus lighting the necessary character. The anode data flow through the display circuit is shown in figures 4-22 and 4-24. The E clock from the I/O microprocessor U3 pin 40 latches the data (AD0-AD7) into the data latch U7. ADR0 and ADR1 are address lines which select one of two anode drivers U9 or U10. After the anode driver is selected, data is strobed into U9 or U10 by the SEG CLK from the I/O decoder U5. The data from the anode drivers is presented to the fluorescent display when the output enable OE line goes low, blanking the display. Each of the 16 anode outputs controls one of the 16 flourescent display segments. When the output goes high (+ 44V) the segment is turned on. When the output goes low (0V) the segment is turned off.

The filament voltage generator U26, U17, Q2 and Q3 (ref: figures 4-22 and 4-25 and Display/Logic schematic sheet 2, coordinates B3) supplies the fluorescent display with a 6 Vp-p square wave that is offset +5V dc. Input to the filament voltage generator is the buffered E clock (BE) from U26 pin 3 (ref: schematic sheet 1, coordinates D5). Push-pull driver, Q2 and Q3, drives the isolation transformer T2.

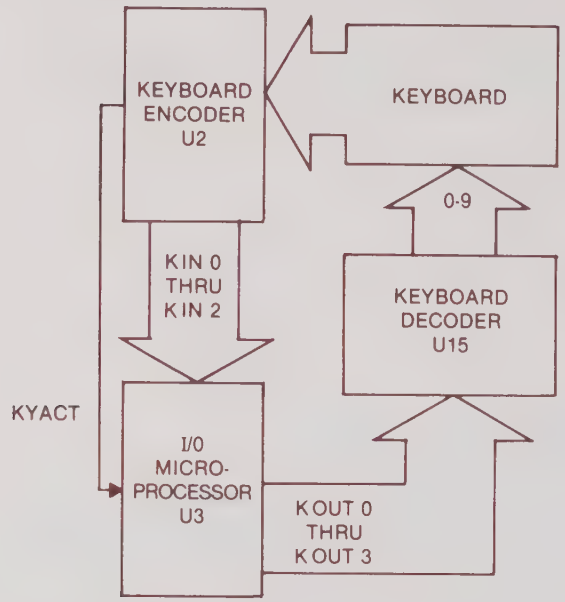


Figure 4-26. Keyboard

4.8.1.3 Keyboard

The keyboard (figures 4-1, 4-26 and Display/Logic schematic sheet 2) consists of 50 membrane switches arranged in a 5 X 10, X-Y matrix. The keyboard Y coordinate is scanned at a predetermined rate by the I/O microprocessor through decoder U15. When a contact is closed, encoder U2 sends a "keyboard is active" signal (KYACT line) to the I/O microprocessor. Microprocessor U3 stops scanning U15 and notes which Y coordinate the count is on. The microprocessor then determines which X coordinates decoded by the I/O microprocessor represent specific actions, parameters, or values.

4.8.1.4 General Purpose Interface Bus

The GPIB interface (ref: figure 4-1, 4-21, 4-27 and Display/Logic schematic sheets 1 and 3) allows the instrument to be remotely programmed by a minicomputer, calculator, etc., via the General Purpose Interface Bus (GPIB). The GPIB interface is an implementation of IEEE Standard 488-1978. It supports the following 488-1978 defined interface functions: Source Handshake (SH1), Accepter Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). This bus transfers messages in byte serial fashion. The bus has 16 signal lines and they are:

8 Data Bus Lines (DIO1 through DIO8)

5 General Interface Management lines (ATN, IFC, SRQ, EOI and REN)

3 Data Byte Transfer Control Lines (NRFD, NDAC and DAV)

These lines are defined in paragraph 3.16, as in operation with the GPIB.

The GPIB interface performs the following two functions:

1. Detects the GPIB Listen and Talk Address.

2. Does the proper listen handshake when attention (ATN) is true.

In the 178, the GPIB interface is controlled by the general purpose interface adapter U1. U1 controls the movement of data between the GPIB bus and the input/output microprocessor. Inputs to U1 from the GPIB are through U13 and U14, bidirectional bus transceivers. U1 data output (AD0-AD7) are connected directly to the I/O microprocessor's data bus. Other lines (R/$\overline{W}$, ADR0, ADR1, ADR2, GPIB/, $\overline{IRQ}$ and E clock) are connected to the I/O microprocessor circuit.

The GPIB address is selected by the GPIB selector switch, located on the rear panel. Switch closures select the GPIB address (Ref: paragraph 2.2.4). The switch contacts are connected to U12 which is a tristate inverter. When G1 and G2 on U12 go low, the inverted GPIB address is placed on the I/O microprocessor's data bus. If G1 and G2 are high, the output from U12 is in a high impedance state.

4.8.1.5 Beeper

The beeper circuit provides an audible indication that a front panel key has been pressed. The beeper may be enabled or disabled by pressing the ♪ (Tone On/Off key.

The beeper sound is created by driving electromechanical transducer DS1 with a burst of 2 kHz pulses for a period of 100 ms.

The beeper circuit (ref: figure 4-28 and Display/Logic schematic sheet 2, coordinates A3) consists of a 12 bit counter U28, the counter control logic U25 pins 8, 9, 10, 5, 6, and 4, the beep driver Q4 and the electromechanical transducer DS1.

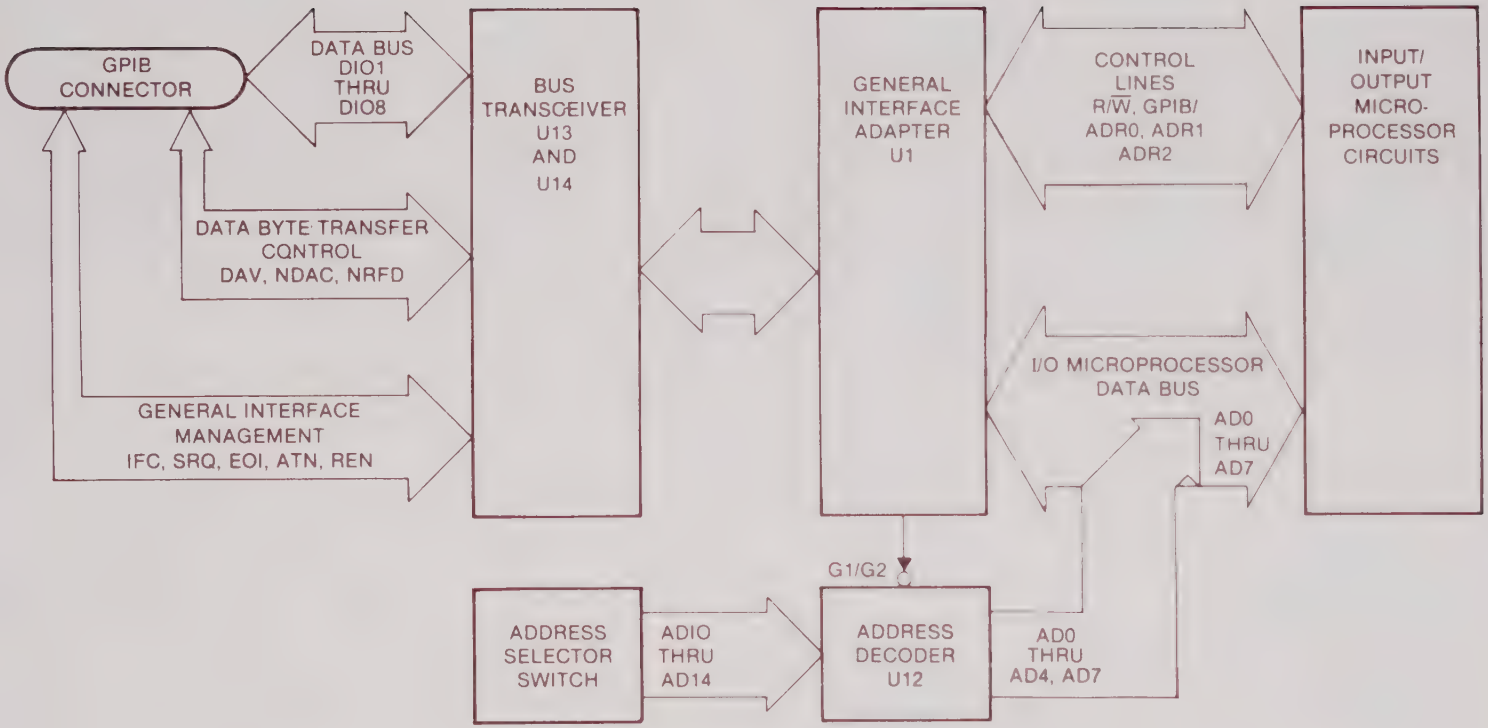


Figure 4-27. GPIB Interface Circuit

The following describes the circuit operation. The counter is reset by the BEEP line, which is generated by the I/O microprocessor U3 pin 20. The counter outputs (Q11 and Q12) U28 pins 1 and 15 are reset to zero; this will enable REC, the serial data from the I/O microprocessor U3 pin 11 to clock the counter at the 62 kHz rate. When the counter outputs Q11 and Q12 both go high, logic gate U25 pin 5 is disabled, which stops the clocking of the counter; this determines the period of the beep. A counter output U28 pin 3 drives the beeper driver Q4 which, in turn, drives the beeper device DS1 at an approximate 2 kHz rate.

4.8.1.6 Optical Isolator

Optical isolation isolates the GPIB ground from the 178 circuit ground.

Actually there are two optical isolator circuits. One optical isolator is located on the front panel assembly and isolates the data received by the I/O microprocessor from the main microprocessor. The second optical isolator is located on the frequency board and it isolates data sent by the I/O microprocessor; it is discussed as part of the main microprocessor.

The I/O microprocessor's optical isolator circuit (ref: figures 4-1 and 4-21, and Display/Logic schematic sheet 1, coordinates C7) consists of optical isolator U24. Serial data is fed into the optical isolator U24 pin 3 on the SERO line that comes from the main microprocessor U42 pin 12 (ref: Frequency Board schematics sheet 3 coordinates D7 and Instrument schematic sheet 1 coordinates A6) through U54 pin 2, J15 pin 20 and J30 pin 20.

4.8.2 Main Microprocessor and Support Circuits

The main microprocessor and support circuits (ref: figures 4-1, 4-29 and Frequency Board schematic sheet 3) act as the central processing unit, they receive optically isolated information from the Input/Output microprocessor (ref: paragraph 4.8.1.1) and act on this input as directed by the software. Software directs the processor to address the subsystems and issue commands and data which directs the 178 to output the desired signal. These subsystems include frequency control logic and control registers on both the Frequency and Output/Power Supply boards.

Software refers to a sequence of commands executed by the main microprocessor. This sequence of instructions stored in Read Only Memory (ROM) com-

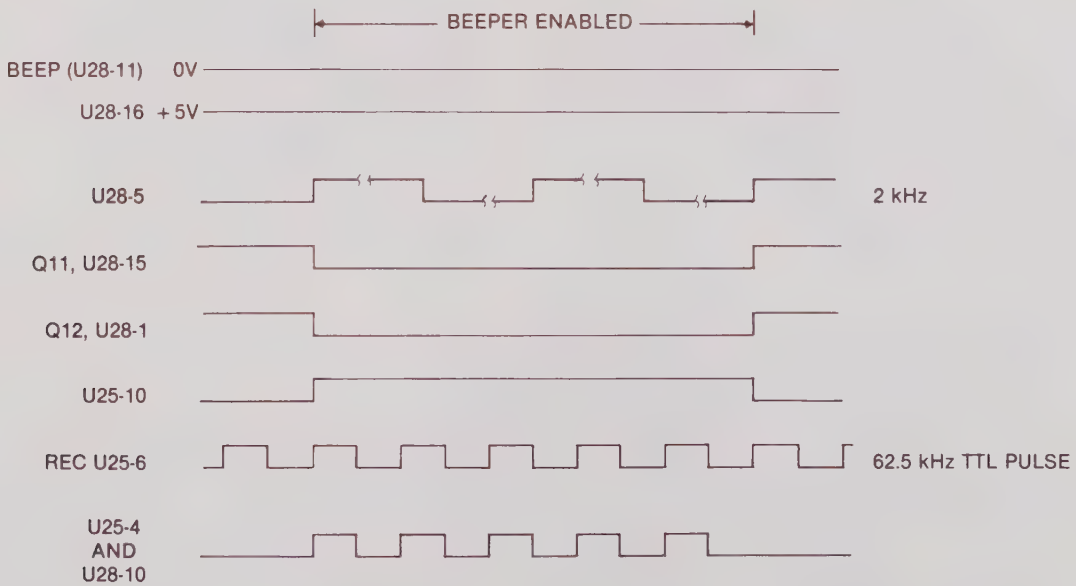


Figure 4-28. Beeper Enabling Circuit Timing (Ref: Display/Logic Schematic Sheet 1)

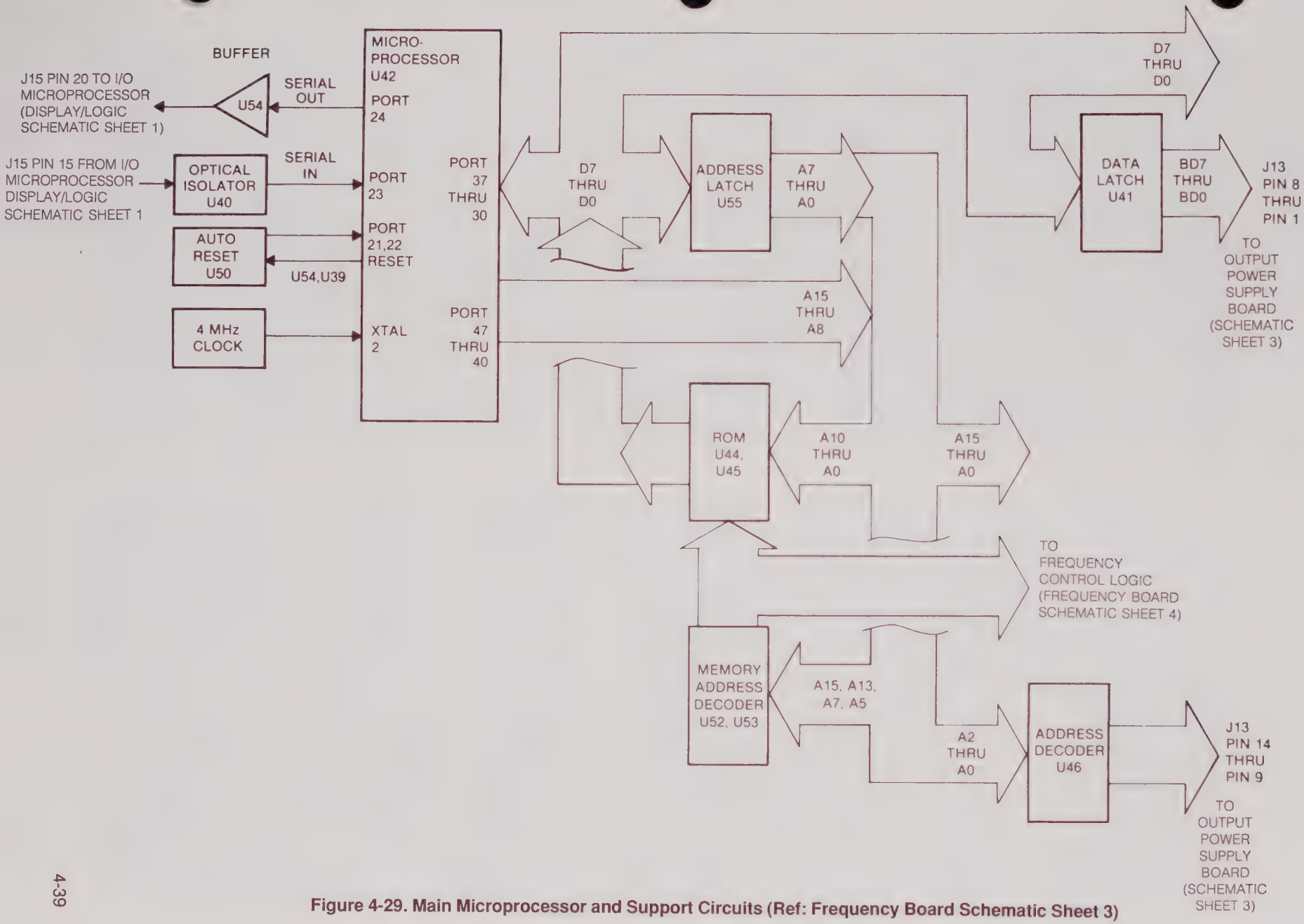


Figure 4-29. Main Microprocessor and Support Circuits (Ref: Frequency Board Schematic Sheet 3)

mands the microprocessor to perform according to the 178 specifications. The microprocessor is powerless without a program to run; therefore, the software is one of the most vital elements of the digital section. All information transfer takes place under the control or supervision of the software. Programs are composed of machine language instructions, messages and tables that provide sequencing information.

The main microprocessor U42 support circuits consist of the address latch, read only memories, memory address decoder, data latch, address decoder, 4 MHz clock, auto reset and optical isolator. The following sections describe each circuit in further detail.

Address Latch The address latch is used to hold the lower order address bits (A0-A7). The address latch U55 (ref: Frequency Board schematic sheet 3, coordinates D6) transfers the data present at its inputs (D0-D7) to its outputs (A0-A7) when the AS line U55 pin 11 goes high.

Read Only Memory The software for the main microprocessor is contained within two Read Only Memories (ROMs), U44 and U45 (ref: Frequency Board schematic sheet 3, coordinates D5). Each ROM receives 10 address lines (A0-A10) from the main microprocessor U42 and the address latch U55. When the memory address decoder U52 enables either ROM, specific address select specific data at the ROM's output (D0-D7). All data from the ROM's are fed as inputs to the main microprocessor.

Memory Address Decoder The memory address decoder U52 and U53 (ref: Frequency Board schematic sheet 3, coordinates C5 and C7) enables the ROM's (U44 and U45), the burst counter U43, the address decoder U46, and portions of the frequency control logic.

The memory address decoder acts upon instructions from the main microprocessor. The memory address decoder is made of three decoder IC's which supply specific output lines (ROM U44, ROM U45, SEL 6840/, WRITEMARKER/, WRITELOAD/, and READFS/) for specific address bytes (A13-A15, A5-A7 and BE).

Data Latch The data latch U41 (ref: Frequency Board schematic sheet 3, coordinates D2) buffers the data from the data bus (D0-D7) of the main microprocessor. The data transfers through the data latch at the positive level of the E clock U41 pin 11, which is supplied by the main microprocessor U42 pin 40. The output data from the data latch (D0-D7) routes through connectors J13 on the frequency board to connector U7 on the output/power supply board (ref: schematic sheet 3).

Address Decoder The address decoder U46 (ref: Frequency Board schematic sheet 3, coordinates C2) provides control commands (ATTN, OFST HI, OFST LO, AMPL and WAVE) to the output/power supply board, control state machine (EP RESET/) and burst counter (INIT BURST/). The decoder select lines (A0-A2) U46 pins 1-3 are decoded when the memory address decoder U53 pin 14 enables the decoder and the E clock, which is supplied by the main microprocessor, U42 pin 40 reaches a positive level. The outputs of address decoder U46 (pins 11-15) are routed through connector J13 pins 9-13 on the frequency board to connector J7 pins 9-13 on the output/power supply board (ref: schematic sheet 3, coordinates A7).

4 MHz Clock The 4 MHz clock is the reference timing source for the main microprocessor system.

The 4 MHz clock originates at the emitter of transistor Q1 (ref: Frequency Board schematic sheet 2, coordinates C1), and it is routed through buffer U59 pin 6 to the XTAL 2 input to the main microprocessor U42 pin 3 (ref: schematic sheet 3, coordinates D7).

Optical Isolator Optical isolation isolates the GPIB ground from the 178 circuit ground.

Actually there are two optical isolator circuits. One optical isolator is located on the front panel assembly and isolates the data received by the I/O microprocessor from the main microprocessor; it is discussed as part of the I/O microprocessor. The second optical isolator is the main microprocessor optical isolator located on the frequency board. It isolates data sent by the I/O microprocessor.

The main microprocessor optical isolator circuit (ref: Frequency Board schematic sheet 3, coordinates D8) consists of an optical isolator U40. Serial data is fed into the optical isolator U40 pin 3 on the SERI line that comes from the I/O microprocessor U3 pin 12 (ref: Display/Logic schematic sheet 1, coordinates C6 and Instrument schematic sheet 1, coordinates A6) through U17 pin 12, J30 pin 15 and J15 pin 15.

Auto Reset The auto reset circuit resets the main microprocessor to the initial power-on conditions (ref: table 2-3, step 3). The auto reset circuit is enabled at power-on or when the auto reset circuit senses an interrupted flow of data from the I/O microprocessor.

The auto reset circuit (ref: Frequency Board schematic sheet 3 coordinates C8) consists of an oscillator U39, a counter U38 and control logic U50 and U54.

The following describes the operation of the auto reset circuit. The microprocessor auto reset circuit resets the main microprocessor when the power is turned on, or when the I/O microprocessor senses an interrupted data flow back to the I/O microprocessor The auto reset circuit is enabled by a pulse at U50 pin 4 from the I/O microprocessor SERIAL IN U42 to pin 11 that resets the 12 bit counter U38. The counter begins to count the 400 kHz clock pulses which are supplied by the oscillator U39. The 12 bit counter counts 4096 cycles then its output, U38 pin 1, will switch to a TTL high, which is inverted by U54 to switch the reset line on the main microprocessor U42 pin 6 low. The reset line is held low while the 12 bit counter counts another 4096 cycles. On the 4096th count, the reset line will switch high to reset the main microprocessor. If the main microprocessor is satisfactorily reset, the serial input data to the main microprocessor, which arrives at a 62.5 kHz rate, will continually reset the 12 bit counter; thus never allowing it to complete its full count (4096). If the main microprocessor will not reset, a single bit on the serial line will again cycle the auto reset circuit until a total of 15 reset cycles have been attempted. At the completion of the 15th cycle, serial communication between the two microprocessors will cease and the display will read PWR ON-ERR RESTART.

4.8.3 Frequency Control Logic

4.8.3.1 Overview

The frequency control logic provides the primary frequency data and phase data for the operation of the frequency synthesizer. It controls operation for single frequency, sweep frequency, phase shift and output marker.

The frequency control logic circuit is shown in figures 4-1, 4-30, and Frequency Board schematic sheet 4. Figure 4-1 shows the frequency control logic and its relationship to the other circuits. Figure 4-30 shows all inputs and outputs, operation and internal data flow of the frequency control logic circuit.

Input data to the frequency control logic circuit comes from the data bus (D0-D7) of the main microprocessor U42 pins 30-37. In addition to the data from the main microprocessor, the frequency control logic receives addresses A0-A3 from the address latch U55.

There are four outputs from the frequency control logic circuit. One output provides data for the divide by N counter in the frequency synthesizer section (ref: paragraph 4.2.2). A second output supplies the data which controls the delay current generator, also within the frequency synthesizer. A third output provides the phase accumulator overflow command to the divide by N counter in the frequency synthesizer. The fourth output supplies the marker output level to the marker output BNC

Figure 4-30 shows internal sections and data flow of the frequency control logic circuit. Each IC is shown controlled by a digital command. The digital commands are described in table 4-4

4.8.3.2 Input

Data input to the frequency control logic circuit is from the data bus (D0-D7) of the main microprocessor. The actual frequency data within the main microprocessor is a 48 bit (binary) word. The 48 bits of frequency data is fed on the data bus (D0-D7) in 8 bit groups. The data is further reduced from 8 bit words to 4 bit words by the frequency data multiplexer U57 and U56 that drives the date input (WRITE DATA 0-3/) to the frequency control logic circuit U70 and U69

4.8.3.3 Data Flow

The data (figure 4-30) is shifted 4 bits at a time into Random Access Memories (RAM) U70, U85, U81, U72, and U80. Next, the data is transferred through latches U86, U90, U79 to the adders U87, U83 and U82

The progression of data through the RAMs, latches, and adders are controlled by commands (table 4-4) from two state machines and addresses from the main microprocessor's address bus (A0-A3).

The ALU state machine (ref: Frequency Board schematic sheet 4, coordinates C2) consists of U66, U67, U64 and U78. This state machine is initiated by the ADD CYCLE from the divide by N counter in the frequency synthesizer. It is clocked by the MCLK1 and MCLK2 from 6.67 MHz clock U59, U60. Its command outputs (STOP, UPDATE FREQUENCY, MSD TIME, LMARK, LDAC AND LDBN) control portions of the frequency control logic. Also, the ALU state machine provides addresses U66 pins 10-13 (AAB0-3) that control portions of the frequency control logic.

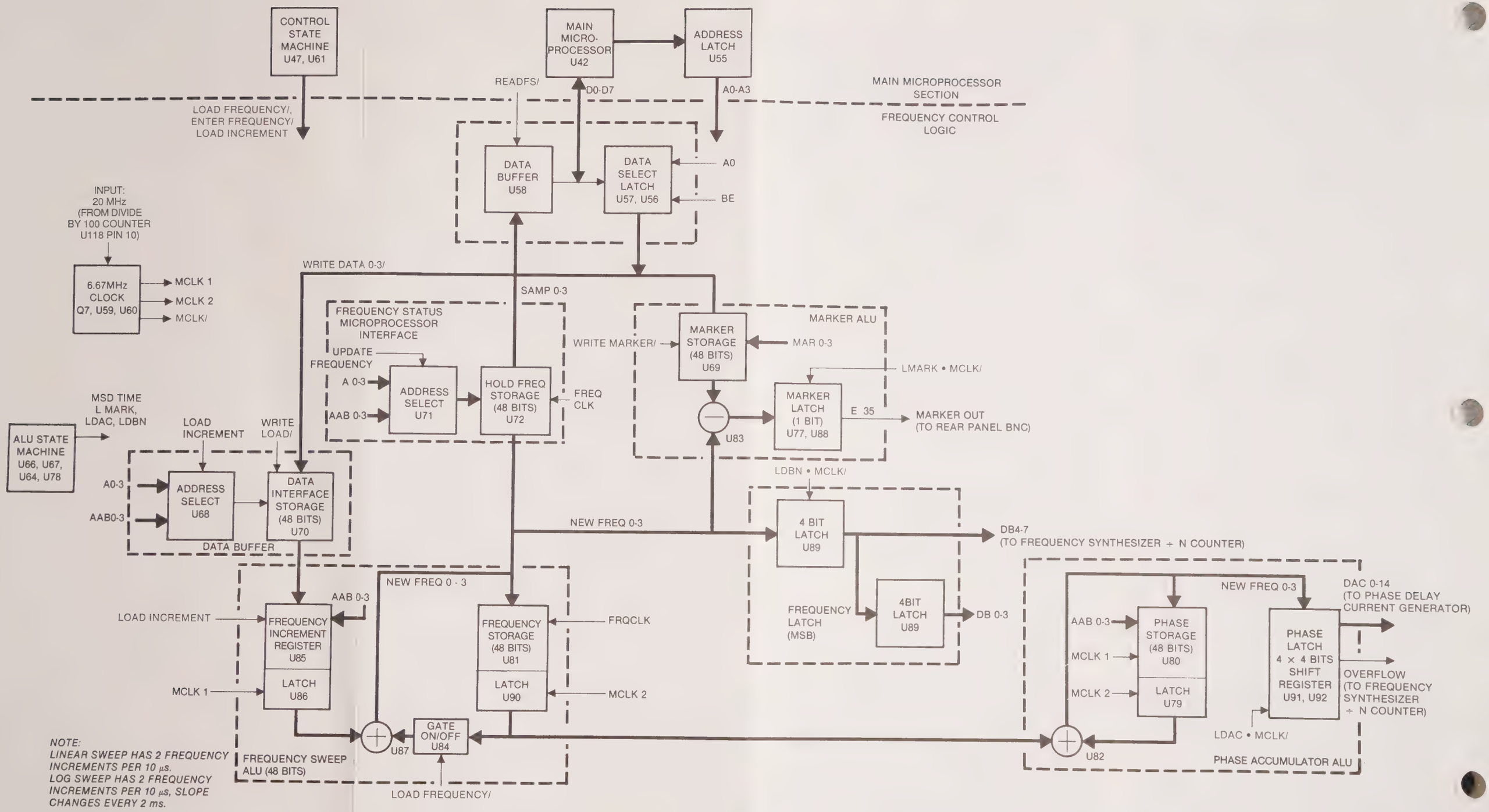


Figure 4-30. Frequency Control Logic Block Diagram (Ref: Frequency Board Schematic Sheet 4)

Table 4-4. Frequency Control Logic Control Commands

Command	Function	Origin	Destination
READFS/	Enables buffer U58 to feed hold frequency data to main microprocessor data bus D0 - D7	Memory address decoder U53 pin 11	Data buffer U58 pin 1 and 19
WRITE LOAD/	Writes data into RAM when a low. Read data when a high	Memory address decoder U53 pin 12	Data interface storage register U7 pin 3
LOAD INCREMENT	Selects either A0 - A3 or AAB0 - AAB3 addresses	Control state machine U61 pin 10	Address selector U68 pin 1
MCLK 1	6.67 MHz clock Inverted MCLK/	6.67 MHz clock U59 pin 2	Frequency increment latch U86 pin 4 and 13
LOAD FREQUENCY/	Enables gate U84 to load frequency data into frequency sweep ALU	Control state machine U61 pin 5	Gate U84 pins 4, 1, 13 and 9
LMARK•MCLK/	Clocks marker output to BNC	ALU state machine LMARK U66 pin 4 and MCLK/ U60 pin 10	Marker latch U77 pin 3
MCLK/•LDBN	Loads 4 most significant frequency bits into divide by N counter	MCLK U60 pin 10 and ALU state machine U66 pin 2	Frequency latch U89 pin 11
WRITE MARKER/	Writes marker frequency data into RAM when low. Reads marker frequency data when high	Memory address decoder U53 pin 13	Marker storage register U69 pin 3
FREQ CLK	Writes NEW FREQ data into RAM when low. Reads frequency data when high	UPDATE FREQUENCY U77 pin 11 and MCLK/ U60 pin 10	Frequency Control storage register U81 pin 3. Frequency hold storage U72 pin 3
MCLK 2	6.67 MHz clock Inverted MCLK/	6.67 MHz clock U59 pin 4	Frequency sweep latch U90 pin 4 and 13
UPDATE FREQUENCY	Selects either A0 - A3 or AAB0 - AAB3 addresses	UPDATE FREQUENCY U77 pin 11	Address selector U71 pin 1

4.8.3.4 Arithmetic Logic Units

The frequency control logic circuit contains three arithmetic logic units (ALU's). These ALU's process data from various sections of the frequency control logic circuit.

The three ALU's, shown in figure 4-30 and Frequency Board schematic sheet 2, are the phase accumulator, frequency sweep and frequency marker ALU's.

Phase Accumulator ALU The phase accumulator controls the pulse delay generator of the frequency synthesizer (ref: paragraph 4.3.2). In addition, the phase accumulator supplies the overflow command to the programmable divide by N counter (ref: paragraph 4.3.2).

The phase accumulator, shown in figure 4-30 and Frequency Board schematic sheet 4, consists of the phase storage register U80, the frequency storage register U81, the data latches U79 and U90, and the adder U82.

There are two data inputs to the phase accumulator U82. One data input comes from the phase storage register U80; the latch U79 provides data isolation between the adder and the phase storage register. The second data input comes from the frequency storage register.

There are two outputs from the phase accumulator adder. The primary outputs are the 4 data bit lines (NEWPH 0-3) that drive both the DAC registers U91 and U92, and the phase storage register. The secondary output is the carry output C1 from U82-9 that is

routed through the DAC register U92 to the programmable divide by N counters overflow input of the frequency synthesizer.

The operation of the phase accumulator is simply adding the contents of two storage registers and replacing the contents of one register with the sum from the adder. Figure 4-31 is an example of how the phase accumulator operates. The contents of the frequency storage register is fixed at 0.125000 in this example; this number does not change when operating in the continuous mode. The contents of the phase storage register depends upon the operation mode of the instrument: for most operations the initial phase data is unimportant, but in order to shift phase (ref: paragraph 3.8.6) the contents of the phase storage register must be modified. For this example the initial phase storage register contents are at 0.222222. In add cycle 1 the two registers are added together and the sum is stored in the phase register, thus replacing the original phase data. The process continues until add cycle 7, when the phase accumulators adder produces a carry output (C1) U82-9. Within the adder loop the carry is dropped and the fractional data is entered into the phase storage register. The add cycles continue.

The phase accumulator continuously operates from power up to power off regardless of the operating mode.

Frequency Sweep ALU The frequency sweep ALU changes the digital frequency data at increments determined by the main microprocessor. This change in frequency data results in a change in frequency.

The frequency sweep ALU, shown in figure 4-30 and Frequency Board schematic sheet 4, consists of the frequency increment register U85, the frequency storage register U81, the data latches U86, U84 and U90, and the frequency sweep adder U87.

There are two data inputs to the frequency sweep ALU. One data input comes from the frequency increment register U85; the data latch U86 provides data isolation between the adder and the frequency increment register. The second data input comes from the frequency storage register U81; data latches U90 and U84 provide data isolation between the adder and the frequency storage register.

The outputs (NEWFREQ 0-3) from the frequency sweep adder U87 are routed to four different sections within the frequency control logic circuit. First, the most significant eight bits are loaded into the latch U89 that controls the frequency synthesizer's pro-

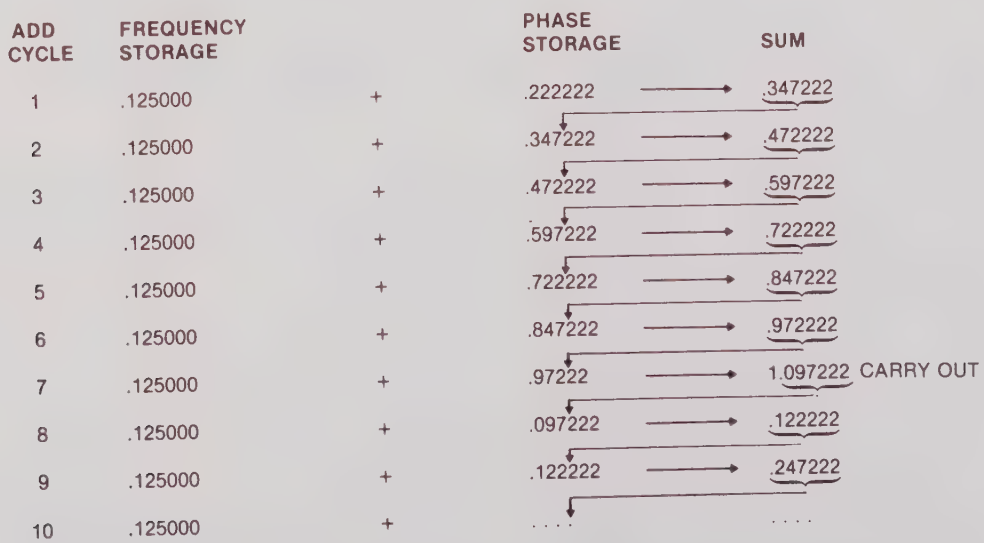


Figure 4-31. Example of Phase Accumulator Adder Cycles

grammable divide by N counter. Second, all 48 frequency bits directly drive one input to the marker ALU. Third, the 48 frequency bits are loaded into the frequency storage register U81 that provides data for the phase accumulator U82. Fourth, the 48 frequency bits are loaded into the data buffer U72 that routes the data back through the main microprocessor to the display, which displays the hold frequency.

The operation of the frequency sweep ALU simply adds the contents of the frequency increment register U85 and the frequency storage register U81 at the frequency sweep adder U87. This sum replaces the contents originally stored in the frequency storage register U81. The frequency sweep adder U87 operates continuously regardless of the instruments operating mode: continuous frequency, linear sweep or logarithmic sweep.

How the instrument sweeps is determined by how the sweep adder processes the increment data. The following sections describe the process for continuous frequency, linear sweep and logarithmic sweep modes.

For continuous frequency, an increment of all zeros is loaded into the frequency increment register U85. Therefore, when the frequency increment is added to the frequency storage data, the sum is unchanged and the frequency will remain unchanged.

In linear sweep mode, an increment, calculated by the main microprocessor U42, is stored in the frequency increment register U85. Every 5 μs the increment is added by U87 to the data stored in the frequency storage register. The sum is then returned to the frequency storage register U81 for the next cycle, thus changing the frequency storage data. The data in the frequency increment register remains unchanged throughout the sweep cycle.

In logarithmic sweep, an increment, calculated by the main microprocessor U42, is stored in the frequency increment register U85. Every 5μs the increment is added to the data stored in the frequency storage register. The sum from the adder is returned to the frequency storage register U81. Every 2 ms the main microprocessor U42 changes the frequency increment. This continuous changing of the increment data causes the frequency to sweep at a logarithmic rate.

Marker ALU The marker ALU provides a level change at the Marker Ouput BNC that indicates when the output frequency equals the selected marker frequency.

The frequency marker ALU, shown in figure 4-25 and Frequency Board schematic sheet 4, consists of the frequency sweep adder U87, the frequency marker storage register U69 and the marker comparator U83.

There are two data inputs to the marker ALU. The first marker ALU input is the data outputs (NEW FREQ 0-3) from the frequency sweep adder U87. The second data input comes from the frequency marker storage register U69. The marker storage register U69 receives its input (WRITEDATA 0-3/) through the main microprocessor U42 from the storage registers U21 and and U22 (schematic 0103-00-1614 sheet 1) associated with the I/O microprocessor.

The output from the marker comparator U83-9 is the carry output C3. From the adder, the carry output is routed to data latch U88-12. When the data latch U88 is clocked (LMARK•MCLK/) the data input is transferred to the Marker Out BNC on the rear panel

The operation of the marker ALU simply compares the contents of the frequency marker storage register U69 and the output from the frequency sweep adder U87. At frequencies less than the selected marker frequency, the carry output will be a TTL low. When the marker frequency and the output frequency are equal, there will be a level transition at the comparator's carry output. The level transition will be either a TTL low to high if the sweep frequency is increasing, or a TTL high to low if the sweep frequency is decreasing. If the sweep frequency is higher than the marker frequency the carry output is a TTL high.

The marker comparator U83 continuously compares the output from the frequency sweep adder U87 to the frequency storage data. As a result, the marker output will always indicate whether the output frequency is greater than or less than the selected marker frequency.

4.9 POWER SUPPLY

The power supply circuits (ref: schematic 0103-00-0752 sheet 4) consist of five voltage regulators: +15V, −15V, +5V referenced to circuit ground and +44V, +5V referenced to isolated (ISO) ground.

All components are located on the output/power supply board except the power transformer on the rear panel. All voltage regulators are series regulators made from discrete components, except the +5 ISO

supply, which is a single linear regulator VR1. The voltage regulators consist of voltage reference sources, operational amplifiers, series pass transistors and current limiting circuits.

The primary circuit reference source is a zener diode CR39 that references the +15V supply. The +15V supply, in turn, is the reference source for the −15V and +5V supplies. The isolated reference source is +5V linear regulator VR1 that is the reference for the +44V ISO and the +5V ISO supplies.

Each voltage regulator has a current limit stage, which protects the power supply from overload conditions. In addition to the current limiting stage, the +5V regulator contains an over voltage protection circuit U36 and Q51 that protects the circuits connected to the +5V line from voltages over a certain limit.

SECTION 5

PERFORMANCE VERIFICATION/CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a Customer Service department. If an instrument is returned to Wavetek for repair or calibration, a detailed description of the specific problem should be attached to minimize turn around time

5.2 PERFORMANCE VERIFICATION

Use this procedure at least once a year to verify instrument performance. If any specification is not met, calibrate the entire instrument. Refer to paragraph 5.3.

5.2.1 Required Test Equipment

Table 5-1 lists the equipment recommended to perform the performance verification (table 5-2). Substitution of any equipment with equivalent or better capability is acceptable.

5.2.2 Verification Procedure

Connect the 178 to the ac power source and allow it to warm up for at least 30 minutes. Use the procedure in table 5-1 to test the instrument performance.

Table 5-1. Verification Test Equipment

Instrument	Suggested Model	Comments
Multimeter	H-P 3478 A	
Universal Counter	H-P 5334A	
Spectrum Analyzer	H-P 8568A	
Synthesizer	Wavetek 178	1, 2, 3 . . ., 9 or 10 MHz, <5 ppm
Oscilloscope		
Mainframe	Tektronix 7904	Bandwidth ≥250 MHz.
Plug-ins		
Dual Trace Amplifier	Tektronix 7A26	
Dual Time Base	Tektronix 7B92A	
Sampler	Tektronix 7S14	
50Ω Terminator	Tektronix 011-0129-00 Tektronix 011-0060-02	50Ω ± 0.1%, 2W

Table 5-2. Performance Verification

Step	Check	Tester	Test Point	Program	Minimum Spec	Maximum Spec
1	Frequency Accuracy (Without Option 002)	Counter	FUNC OUT (Use 50Ω Termination)	Reset FREQ: 1E7	9.99995 MHz	10.00005 MHz
2				FREQ: 499.99999	499.99749 Hz	500.00249 Hz
3	Frequency Accuracy (With Option 002)			FREQ: 1E7	9.9999995MHz	10.0000005MHz
4				FREQ: 499.99999	499.9999749Hz	500.0000249Hz
5	Amplitude Accuracy	Oscilloscope Plug-Ins 7A13 7B92A		FREQ: 1E3 AMPL: 10	9.89V	10.11V
6				FUNC: 1	9.79V	10.21V
7				FUNC: 2		
8				FUNC: 3	9.39V	10.61V
9	Offset Accuracy			FUNC: 2	-0.14	0.14
10				FUNC: 1		
11				FUNC: 0		
12	Amplitude Resolution	Multimeter (Vrms)		AMPL: 2.56	892 mV	918 mV
13				AMPL: 1.28	444 mV	461 mV
14				AMPL: 1.29	447 mV	465 mV
15				AMPL: 1.30	451 mV	468 mV
16				AMPL: 1.32	458 mV	475 mV
17				AMPL: 1.36	470 mV	490 mV
18				AMPL: 1.44	500 mV	518 mV
19				AMPL: 1.60	556 mV	575 mV
20				AMPL: 1.92	668 mV	690 mV
21	DC Voltage Accuracy	Multimeter (Vdc)		FUNC: 4 AMPL: 0 OFST: 10.00	9.860V	10.140V
22				OFST: -10.00	-10.140V	-9.860V
23				OFST: 5.00	4.910V	5.090V
24				OFST: 2.56	2.494V	2.625V
25				OFST: 1.00	0.950V	1.050V
26				OFST: -1.00	-1.050V	-0.950V
27				OFST: 0	-40mV	+40mV
28				OFST: 1.28	1.227V	1.332V
29				OFST: 1.29	1.23V	1.34V
30				OFST: 1.30	1.24V	1.35V
31				OFST: 1.32	1.26V	1.37V
32				OFST: 1.36	1.30V	1.41V
33				OFST: 1.44	1.38V	1.49V
34				OFST: 1.60	1.54V	1.66V
35				OFST: 1.92	1.86V	1.98V
36	Attenuator Accuracy			FUNC: 4 OFST: 0 AMPL: 4.0	3.95V	4.05V
37				AMPL: 0.4	0.386V	0.414V
38				AMPL: 0.04	0.038V	0.042V
39				AMPL 0.004	0.00378V	0.00422V

Table 5-2. Performance Verification (Continued)

Step	Check	Tester	Test Point	Program	Minimum Spec	Maximum Spec
	For steps 40 through 42, record the indicated items at the worst case harmonic (typically the second or third)					
40	Sine Distortion	Spectrum Analyzer Settings: State; Preset Atten; 30 dB Ref Level; 0 dB Mixer Level; -30 dBm Start Freq; 1.2 X Freq. Stop Freq; 3.5 X Start freq.	Connect rear panel "FUNC OUT" through X5 atten. to analyzer "100 Hz-1.5 GHz INPUT". Connect front panel "FUNC OUT" to analyzer "100 kHz-1.5 GHz INPUT".	AMPL: 2.82 FREQ: 5kHz to 50kHz in 5kHz Steps	Fundamental: Frequency; _____ kHz Amplitude; _____ dBm Harmonic: Amplitude; _____ dBm	
				(Harmonic Amplitude must be at least 55 dBm below the Fundamental Amplitude)		
41				FREQ: 50kHz to 300kHz in 50kHz Steps FREQ: 300kHz to 500kHz in 20kHz Steps	Fundamental: Frequency; _____ kHz Amplitude; _____ dBm Harmonic: Amplitude; _____ dBm	
				(Harmonic Amplitude must be at least 40 dBm below the Fundamental Amplitude)		
42			FUNC OUT (Use 50Ω Termination and) X5 Atten.	FUNC: 0 FREQ: 5MHz to 50MHz in 5MHz Steps, and at 27.5MHz	Fundamental: Frequency; _____ kHz Amplitude; _____ dBm Harmonic: Amplitude; _____ dBm	
				(Harmonic Amplitude must be at least 30 dBm below the Fundamental Amplitude)		
43	Spurious Level	Spectrum Analyzer Settings: Preset Ref. Level; 20dB Span; 20kHz Center Freq; 1.005 MHz		FREQ: 1005E3	All spurs at least 44 dBc below fundamental	
44		24.005 MHz		FREQ: 24005E3		
45		48.005 MHz		FREQ: 48005E3		
46	Rise/Fall Time (Measured between 10 and 90% points) and Aberrations	Oscilloscope Plug-In 7S14		FREQ: 6E6 FUNC: 2 AMPL: 20	Rise/Fall Time Aberrations	≤12ns (Each transition) ≤5% ± 50 mV (Of peak to peak voltage)
47				AMPL: 10	Rise/Fall Time	≤10ns (Each transition)
48				AMPL: 5	Aberrations	≤5% ± 50 mV (Of peak to peak voltage)

Table 5-2. Performance Verification (Continued)

Step	Check	Tester	Test Point	Program	Minimum Spec	Maximum Spec
49	Trigger Baseline (Without Trigger Input)	Multimeter (Vdc)	FUNC OUT (Use 50Ω Termination)	FREQ: 200kHz AMPL: 10 MODE (Main): 1 FUNC: 0	-100mV	100mV
50				MODE (Main): 4	-5.1V	-4.9V
51	Trigger Baseline (With Trigger Input)	Counter		MODE (Main): 0	199.9kHz	200.1kHz
52				MODE (Main): 1 (Connect 10.1kHz sine wave to TRIG IN connector)	10.05kHz	10.15kHz
53				MODE (Main): 2	100.5kHz	101.5kHz
54				MODE (Main): 3 BURST Count: 7	70.35kHz	71.05kHz
55				MODE (Main): 4	10.05kHz	10.15kHz
56				MODE (Main): 5	100.5kHz	101.5kHz
57				MODE (Main): 6 BURST Count: 7	70.35kHz	71.05kHz
58	AM Input	Multimeter (Vrms)		MODE: 0 FUNC: 5 (Connect 0Vdc to AM IN connector)	Record Results (Should be approximately 5Vp-p)	
59				Step AM IN from -3.5Vdc to -2Vdc in 0.1Vdc steps	Record AM IN dc voltage corresponding to an output voltage of -0.1 to +0.1V	
60				Step AM IN from 2Vdc to 3.5Vdc in 0.1Vdc steps	Record AM IN dc voltage corresponding to an output voltage of >2X Step 89 Results	
61		Calculation		Step 91 Results-Step 90 Results	4.752V	6.048V
62	Reference Input/ Output	Counter Signal Source Func; Square Ampl; 2.5V Freq; 999.993 kHz	REF OUT Connect Signal Source "Function Out" to 178 under test "REF IN"	Reset	999.993 kHz	(No deviation)
63		Signal Source Freq change 1.000007MHz			10.00007 MHz	(No deviation)
64		Signal Source Freq change 9.99993 MHz			9.99993 MHz	(No deviation)
65		Signal Source Freq change 10.00007MHz			10.00007MHz	(No deviation)

Table 5-2. Performance Verification (Continued)

Step	Check	Tester	Test Point	Program	Minimum Spec	Maximum Spec
66	Linear Sweep Start Voltage/Freq.	Connect; SWEEP OUT to DMM	See "Tester" column	SWEEP MODE: 3 Trig. Linear Ramp	-100 mVdc 9.999 kHz	+100 mVdc 10.001 kHz
67	Linear Sweep Stop Voltage/Freq.			START FREQ: 10 kHz	4.5 Vdc 19.999 kHz	5.5 Vdc 10.001 kHz
68	Log Sweep Start Frequency	SYNC OUT to Counter		STOP FREQ: 20 kHz	9.999 kHz	10.001 kHz
69	Log Sweep Stop Frequency			SWEEP TIME: 0.01 Use "MAN TRIG" to initiate sweep	19.999 kHz	20.001 kHz
70	Sweep Time	Counter	FUNC OUT (Use 50Ω Termination)	Reset FREQ: 200 kHz AMPL: 2.5 FUNC: Square MODE: Trig TRIG Mode: INT SWEEP TIME: 1234 ms	1233.9 ms	1234.1 ms
71				Sweep Time; 43.21 ms	43.205 ms	43.215 ms
72	Marker/Output Status	Multimeter (Vdc)	MARKER OUT (TTL)	Reset FREQ: 999.99 Hz	0 V	0.5 Vdc
73				FREQ: 5000.01 Hz	2.5V	5.0V
74				MARKER #: 10 MARKER FREQ: 5 kHz MAIN FREQ: 4.99999 kHz	0 V	0.5 Vdc
75				MAIN FREQ: 5.00001 kHz	2.4 Vdc	2.5 Vdc

5.3 CALIBRATION

Table 5-3 lists the equipment required to perform the calibration procedures given in table 5-4. Out-of-spec operation, replacement or repair of the Frequency or Output/Power Supply board will require complete recalibration of the instrument. If the reference board is repaired or replaced, it may be calibrated by using steps 6, 7, 8 and 13 without adjustment to the other boards.

> *NOTE*
>
> *The completion of the calibration procedure returns the instrument to correct alignment.* ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS*** *Instrument specifications are given in section 1 of the standard Model 178 instruction manual.*

Periodic calibration of all boards is needed because of component aging, which depends on instrument on-time and environment. Use six months as an initial calibration period. If possible, keep records of the parameter values, and modify the time between calibrations if the records indicate.

For access to the board assemblies, remove the six screws securing the top cover and six screws securing the bottom cover, then remove the covers. For access to the shielded portion of the Reference Board, remove the four screws securing the module cover and lift the cover off the module. (Ref: chassis drawing sheet 2.)

The VCO, Display Logic, Rear Panel, Stored Setting boards do not require calibration.

NOTE

1. EXEC (Execute), required to implement parameter value change, has been omitted from the calibration procedures. If there is any question about 178 operation, refer to section 3.

2. When using the Function Out BNC, it must be terminated with a 50Ω load.

5.4 FAN FILTER

The air inlet for the instrument cooling fan contains a filtering screen that must be cleaned periodically. To clean, remove the screen retainer and screen (at the rear of the instrument). Vacuum or wash and dry the screen as necessary (at least yearly).

Table 5-3. Calibration Test Equipment

Instrument	Suggested Model	Comments
Digital Voltmeter	Fluke 8520A	True rms ac option.
Peak Detector	Tektronix 067-0625-00	
Frequency Counter	Hewlett-Packard 5370A	>50 MHz 0.00005% accuracy.
Oscilloscope		
Main Frame	Tektronix 7904	Bandwidth ≥250 MHz.
Plug-Ins		
Dual Trace Amplifier	Tektronix 7A26	
Dual Time Base	Tektronix 7B92	
Differential Comparator	Tektronix 7A13	
Sampler	Tektronix 7S14	
Probe	Tektronix P6106	× 10

Table 5-3. Calibration Test Equipment (Continued)

Instrument	Suggested Model	Comments
Spectrum Analyzer	Hewlett-Packard 8568A	
Coax-to-BNC Adapter		Female BNC, 6-inch, 50Ω coax cable and male portion of vertical coax connector for circuit boards.
Load		50Ω ±0.1% 15W
Attenuator		50Ω × 5, 2W
Reference Frequency Generator	Wavetek 178	1, 2, 3 . . ., 9 or 10 MHz, <5 ppm
Function Generator	Wavetek 182A	1 kHz, 5 Vp-p Triangle

Table 5-4. Calibration Procedure

NOTE: Open column indicates previous entry remains applicable.

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	+15V Supply Voltage	DVM (dc mode)	FB2, TP6 (Gnd) (Output/Power Supply)	RESET	R307 (Output/ Power Supply)	+15 ± .01V	Use TP6 for ground.
2	−15V Supply Voltage		FB3, TP2 (Gnd) (Output/Power Supply)		None	−15 ± .05V	Verify
3	+5V Supply Voltage		FB1, TP6 (Gnd) (Output/Power Supply)			+5.19 ± .02V	Verify
4	+5V ISO Supply Voltage Ground Reference		J8-3 (+5 ISO) J8-2 (Gnd) (Output/Power Supply)			+5 ± 0.2V	Verify Use J8-2 for ground.
5	+44V ISO Supply Voltage		J8-1 (+44V ISO), J8-2 (Gnd) (Output/Power Supply)			+44 ± 2V	
6	100 MHz Reference Spurious	Spectrum Analyzer Center Freq: 100 MHz Freq Span: 50 MHz	J3 (Reference Board). Connected with coax-to-BNC adapter.	After test connection is made POWER: ON	C41 and C45 (Reference Board)	7Vp-p, spurious >65 dBc	Remove cable from J3 (Reference Bd) and with coax-to-BNC adapter, connect analyzer to J3. Display will be blank.
7	100 MHz Reference Level				C53 (Reference Board)	Level ⩾+2dBm	After adjustment, reconnect cable to J3.

Table 5-4. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
8	Mixer Spurious	Spectrum Analyzer Center Freq: 50 MHz Freq Span: 5 MHz Res BW: 30 kHz Sweep Time: 20ms Attn: 20 dB Video BW: 30 kHz	FUNC OUT (Front Panel BNC)	FREQ: 49E6	R282 (Frequency Board)	51 MHz spurious to minimum value. (Typically >65 dBc).	49 MHz, 1Vpp sine wave at FUNC OUT.
9	Fractional Frequency Spurious	Spectrum Analyzer Center Freq. 1.005 MHz Freq Span: 20 kHz Res BW: 300 Hz Sweep Time: 1 sec Attn: 20 dB		FREQ: 1.005E6	R134: Coarse adjust. R139: Fine adjust. (Frequency Board)	Adjust spurious to >50 dBc	
10	24M Spurious	Spectrum Analyzer Center Freq: 24.005 MHz		FREQ: 24.005E6	R144 (Frequency Board)		
11	48M Spurious	Spectrum Analyzer CENTER FREQ: 48.005 MHz		FREQ: 48.005E6	R151 (Frequency Board)		
12	Pulse Width Adjustment in Reference Input Circuit	Oscilloscope with × 10 Probe WWV Broadcast 1 MHz Freq Standard. Amplitude: 1 Vp-p Connect ref signal to EXT REF IN	U1-4 (Reference Board)	FREQ: 1E6	R25 (Reference Board)	Display will read "REF LOCKED". Pulse width 70 ± 10ns (See figure 5-1).	If in sync, "REFERENCE LOCKED; will display. If not, "REFERENCE NOT LOCKED" will display.
13	Low Frequency Mixer Zero	Disconnect WWV Freq Standard. DVM (dc mode)	TP1 and TP7 (Gnd). (Output Power Supply Board)	RESET	R41 (Output/ Power Supply Board)	0 ±.002V	

NOTE: Center R279 before performing next step.

14	DC Offset DAC Zero	DVM (dc mode)	TP4 and TP8 (Gnd) (Output/Power Supply/Board)	RESET	R271 (Output/ Power Supply Board)	0 ±.002V	
15	Power Amplifier Zero		FUNC OUT Front Panel, into 50Ω Load	FUNC:4 AMPL: 0	R174 (Output/ Power Supply Board)		
16	Pre-amplifier Zero			AMPL: 10	R143 (Output/ Power Supply Board)		Repeat steps 15 and 16 once.

Table 5-4. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
17	Trigger Baseline Zero	DVM (dc mode)	FUNC OUT Front Panel, into 50Ω Load	RESET MODE (Main): 1	R17 (Frequency Board)	0 ±0.005V	
18	DC Voltage level			RESET OFFSET: 4 AMPL. 0 FUNC:4	R273 (Output/ Power Supply Board)	+4 ±0.004V	50Ω Load required
19	Voltage Level Balance			OFFSET: −4	R279	Split Error between positive and negative offset	After completion of this step, repeat step 18 once
20	Verify Negative DC Voltage Level				No Adjustments	−4V ± .004Vdc	If desired results are not achieved, repeat steps 18, 19 and 20.
21	Sine Wave Amplitude	DVM (ac mode, true rms)	FUNC OUT Terminate into 50Ω load.	RESET FREQ: 5E3 AMPL: 10	R4 (Output/ Power Supply Board)	3.535 Vrms ± 0.01 Vrms	10Vp-p Sine Wave
22	Triangle Balance	DVM (dc mode)		FUNC: 1 FREQ: 1E3	R86 (Output/ Power Supply Board)	0V ± 10 mV	R86 adjusts offset.
23	Triangle Peaks	Oscilloscope			R87 (Output/ Power Supply Board)	Adjust for sharp peaks.	
24	Triangle Amplitude	Oscilloscope with 7A13 Plug-in			R91 (Output/ Power Supply Board)	Triangle 10 Vp-p ± 20 mV	Triangle is 10 Vp-p
25	Triangle Offset	DVM (dc mode)			Verify, Adjust R86 if not correct	0V ± 110 mV	If R86 is adjusted repeat steps 22 through 24.
26	Ramp Amplitude	DVM (ac mode)		FUNC: 3	Verify	2.94 Vrms ±40 mV	If condition cannot be met, repeat steps 22 through 25.
27	Ramp Offset	DVM (dc mode)			Verify	0 ±0.2V	

Table 5-4. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
28	Square Wave Negative Peak	DVM (dc mode)	FUNC OUT Terminate into 50Ω load.	FUNC: 2 FREQ: .05	R115 (Output/ Power Supply Board)	−5 ±0.01V	50 mHz, 10 Vp-p square wave.
29	Square Wave Positive Peak				R121 (Output/ Power Supply Board)	+5 ±0.01V	
30	AM Offset (Modulated)	DVM (dc mode) and function generator. Function generator output 1 kHz approx. 5 Vp-p (offset < ±5 mV), connected to AM IN BNC.		RESET. FUNC: 5 AMPL: 10 Vp-p FREQ: 1E5	R68 Amplitude (Output/ Power Supply Board)	0V ±50 mV	
31	AM Balance	Oscilloscope			R61 (Output/ Power Supply Board)	Symmetrical Modulation Envelope. See figure 5-2.	
32	AM Amplitude	DVM (ac mode). Remove 1kHz sine from AM IN.		FREQ: 5E3	R55	1.768 Vrms ± 10 mV	
33	AM Offset (Unmodulated)	DVM (dc mode)			None	0V ± 110 mV	If condition cannot be met, repeat steps 30 through 32.
34	Wave Symmetry	Sampling Scope	FUNC OUT Terminate with X5, 50Ω Attenuator.	RESET. MODE (Sweep): 3 START FREQ: 1E6 STOP FREQ: 50E6 TIME: 20 FUNC: 2 AMPL: 8Vpp	R292 (Frequency Board)	50 ± 1% duty cycle	Adjust R292 for 50% sym. at 1 MHz prior to pressing MAN TRIG in step 35.
35				MAN TRIG	No adjustment	50 ± 10% duty cycle	Generator is sweeping 1 to 50 MHz.

Table 5-4. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
36	Wave Symmetry	Sampling Scope	FUNC OUT Terminate with X5, 50Ω Attenuator	MAN TRIG	R301	50% ± 5% duty cycle	Generator frequency is at 50 MHz. After completing this step, repeat steps 32 through 34 once.
37	Square Wave Rise/Fall Time and Aberrations			RESET. FREQ: 6E6 FUNC: 2 AMPLITUDE: 8 Vp-p	C98, R198 (Output/ Power Supply Supply Board)	Rise/Fall time ⩽10 ns Aberrations ⩽5% of peak to peak voltage. See figure 5-3	
38	Sine Amplitude Temperature Compensation	DVM (dc mode)	TP6 and TP2 (Gnd) (Frequency Board)	RESET.	R224 (Frequency Board)	+11V ±1.5 Vdc	
39	Frequency Response	DVM (dc mode, 200 mV full scale range) with Peak Detector. Set up as shown in figure 5-4.	FUNC OUT Terminate with a X5, 50Ω Attenuator connector to Peak Detector.	FREQ. 5E3 AMPL: 6Vp-p	Use ↑ or ↓ key to adjust LSB of amplitude	0V ±2 mV	Note Reference Level
40				FREQ. 501E3	R229 (Frequency Board)	Reading in step 40 ±2mV	
41				FREQ: 42. 5E6	C49 (Output/ Power Supply Board)	Reading in step 40 ± 10 mV	
42				FREQ: 500 E3	None	Reading in step 40 ± 30 mV	If bad, refer to table 6-5.

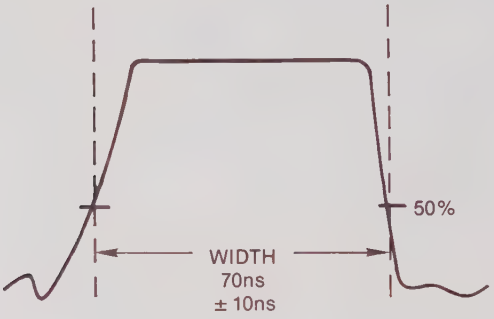


Figure 5-1. Width

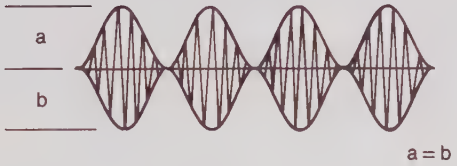
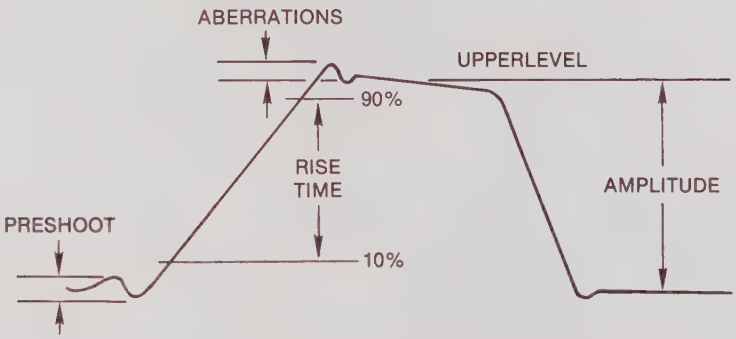


Figure 5-2. Symmetrical Modulation Envelope



NOTE: THIS EXAMPLE IS EXAGGERATED FOR ILLUSTRATION PURPOSES.

Figure 5-3. Aberrations

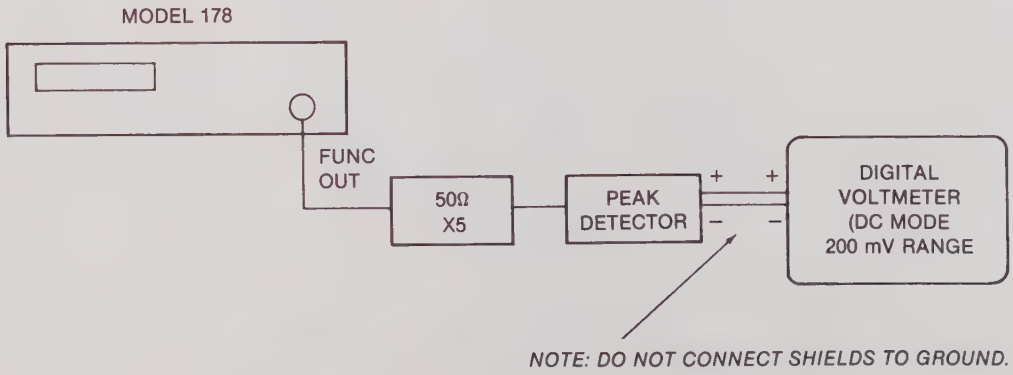


Figure 5-4. Frequency Response Test Setup

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for alignment or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU SHART

CAUTION

To prevent damage to components, turn unit off while removing or replacing components, connectors or PC boards.

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this section is to give guidance for the most likely problems the user may encounter.

Table 6-1 lists the symptom recognition tables. These tables direct the user to the functional area of the instrument for general output problems. Table 6-2 lists tables that supply voltages, state conditions, and waveforms for troubleshooting functional parts, and timing diagrams for several key digital sections.

If you suspect microprocessor or programming problems internal to the 178, we recommend the instrument be returned to the factory, since software and certain digital information are not included in this guide.

Table 6-1. General Output Problems

Table	Title
6-3	Waveform Problems
6-4	Amplitude Problems
6-5	Amplitude Response Problems
6-6	DC Offset Problems
6-7	Frequency Problems

Table 6-2. Voltage and Waveform Tables

Table	Title
6-8	+ 15V Regulator
6-9	− 15V Regulator
6-10	+ 5V Regulator
6-11	+ 5V Isolated Regulator
6-12	+ 44V Isolated regulator
6-13	Triangle Converter
6-14	AM Circuit
6-15	Sync and Square Wave Shaper
6-16	Preamplifier
6-17	Binary Attenuator
6-18	Power Amplifier
6-19	Output Attenuator
6-20	DC Offset
6-21	Function Control Logic
6-22	Low Frequency Mixer
6-23	Frequency Reference
6-24	Synthesizer Phase Lock Loop
6-25	Delay Generator
6-26	High Frequency Spurious Compensation
6-27	Mixer and Buffer Amplifier
6-28	Divide By 100 Counters
6-29	Trigger Slope and Source Control Logic
6-30	VCO

6.3 STARTING

When confronted with a problem, initially check the power supplies (table 6-8 through 6-12). Once the power supplies are determined to be good, use the appropriate tables for isolation. This information in conjunction with circuit descriptions (section 4), schematics (section 7), and figure 4-1 should be useful in determining most field problems.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.

2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.

3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500mV forward voltage (or reversed bias), the transitor is defective.

4. A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).

5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.4.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.

2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.

3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.

2. The gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

3. If the device supplying gate voltage to an FET saturates, the FET has too large a Vgs (pinch off) for the circuit and should be replaced.

6.4.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.

2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.4.6 Digital TTL IC's (e.g. 7400 Series)

1. The device is operating correctly if the output high state is $> +2.4V$ and low state is $< +0.5V$.

2. The input must show the same two levels as in step 1. If the levels are between $+0.8V$ and $+2.0V$, the connection to the driving circuit output is open.

Table 6-3. Waveform Problems

Problem	Probable Cause	Solution
1. No waveform output, distored waveforms. SYNC OUT is normal.	Problem is in the preamp, binary attenuator, power amplifier or output attenuator.	Reset the generator. Check for 1 kHz sine output at output of preamp and power amplifier. Check for proper switching logic in the binary and output attenuators. See tables 6-17, 18 and 19.
2. Square waveform problem only. SYNC OUT is normal.	Problem is in square wave shaper circuit.	Check sync and square wave shaper U7, Q17, CR15, CR16, U21 and associated circuitry (0103-00-0752 sheet 2). See table 6-15.
3. No square waveform and SYNC OUT at all frequencies.	1. Square wave cable is not properly connected or square wave amplifier U36 problem (see problem 9).	1. Check connector J10 on frequency board (0103-00-0949 sheet 2).
	2. Square wave level detector is malfunctioning.	2. Check level shifting circuitry U117, Q37, U38, U37, and associated circuitry (0103-00-0949 sheet 7). See table 6-27.
4. No square waveform for frequency <500 kHz.	Square divide-by-100 counter problem.	Check U27, U21, U20, U23, U11, U19, U6 (0103-00-0949 sheet 1). See table 6-28.
5. No sine wave for frequency >500 kHz.	1. High frequency sine wave cable is not properly connected.	1. Check connector and cable at J9, near mixer buffer amplifier (0103-00-0949 sheet 7).
	2. Sine wave filter and switch problem.	2. Check L7-L9, C45-C48, (0103-00-0752 sheet 2) and K1 (0103-00-0949 sheet 7).
6. No sine wave for frequency <500 kHz. Also no triangle wave.	Program frequency to 100 kHz. Check for 1 MHz signal at E6 and 1.1 MHz at E8 (0103-00-0752 sheet 1). E8 originates at J12 from U4 (0103-00-0949 sheet 1).	
	1. If no 1 MHz, 100 MHz ÷ 100 counter problem.	1. Check 1 MHz delay circuit (0103-00-0949 sheet 1). If no output, check the 100 MHz ÷ 100 counter (0103-00-0949 sheet 2). See table 6-28.
	2. If 1.1 MHz, variable frequency ÷ 100 counter problem.	2. Check 1.1 MHz output from U3 and U4 (0103-00-0949 sheet 1). If no output check the variable frequency ÷ 25 counter. See table 6-28.
	3. If otherwise, low frequency (LF) mixer problem.	3. Check the LF mixer circuit (0103-00-0752 sheet 1). See table 6-27.
7. Triangle wave problem.	Triangle converter circuit.	Check triangle converter U8, U9 (0103-00-0752 sheet 2). See table 6-13.

Table 6-3. Waveform Problems (Continued)

Problem	Probable Cause	Solution
8. AM signal problem.	AM circuit.	Check AM circuit Q9-Q12, U6 (0103-00-0752 sheet 2). See table 6-14.
9. Waveform output does not agree with display.	Waveform selection logic and switch problem.	Check function control logic and switches (0103-00-0752 sheet 2) according to table 6-21.
10. Ramp waveform excessive overshoot or retrace.	Q7 or U26 is defective.	Q7 should be on when ramp is selected, off for other waveforms (0103-00-0752 sheets 1 and 3).
11. Ramp waveform retrace does not coincide with peak voltage.	Square wave synchronization logic malfunction.	Check U10-U13, U18, U20, U22 (0103-00-0949 sheet 1).

Figure 6-4. Amplitude Problems

Problem	Probable Cause	Solution
1. Amplitude range not accurate.	Resistor network in output attenuator is defective.	Check for defect, short circuit or wrong value components R243-R268 (0103-00-0752 sheet 3).
2. Amplitude ranging is not correct.	Relay or control logic in output attenuator is malfunctioning.	Check K4-K10 and the control logic (table 6-19). Check if C110 is shorted.
3. Amplitude accuracy and resolution problem.	1. Binary attenuator problem. 2. Shorted capacitor.	1. Check switch logic (table 6-17). Program amplitude to 0.00V and check R152-R157, R159, R160, R162, R163, R165, R167, R168, R170, R352-R356 with ohm meter. 2. Check C77, C241 and C242 for short.
4. Sine amplitude at <kHz too low.	Half of the low frequency mixer is not functioning.	Check for defective U2, U3, Q5 or Q6 (0103-00-0752 sheet 1). See table 6-22.

Table 6-5. Amplitude Response Problems

Problem	Probable Cause	Solution
1. Excess rolloff at 50 MHz, both sine and square waves. (continued on next page)	1. Output amplifier problem.	Check for open capacitor in the power amplifier (0103-00-0752 sheet 3), especially C85-C90. Check for defective C110, C97, C98, R241. See table 6-18.

Table 6-5. Amplitude Respnse Problems (Continued)

Problem	Probable Cause	Solution
1. Excess rolloff at 50 MHz, both sine square waves. (continued)	2. Preamplifier problem.	Check for defective capacitors in preamp, R133 and R137. See table 6-16.
	3. Defective filter components.	L7-L9, C45-C48 (0103-00-0752 sheet 3). Also L4-L6, C135-C138 (0103-00-0949 sheet 7).
	4. Defective mixer buffer amplifier.	Check for defective capacitors in the buffer amplifier (0103-00-0949 sheet 7). See table 6-27.
2. Excess rolloff at 500 kHz sine wave.	Defective filter.	Check for defective components, L4-L6, C22-C25 (0103-00-0752 sheet 1). Notch filter Q7 (0103-00-0752 sheet 1) should not be on except when ramp waveform is selected.

Figure 6-6. DC Offset Problems

Problem	Probable Cause	Solution
1. Output offset is not zero when program offset to zero.	1. Preamp problem if its output is not zero.	1. Check for defective U10, R143 and the associated circuit (0103-00-0752 sheet 2). See table 6-16.
	2. DC offset circuit is malfunctioning if U29-6 is not zero.	2. Check for defective U27, U28, U29 and U30 (0103-00-0752 sheet 3). Check also the control logic U25, U26 and U27. See table 6-20.
	3. Power amplifier problem.	3. Check for correct dc bias voltage (table 6-18 and 0103-00-0752 sheet 3).
2. Output offset for frequency >500 kHz.	C141 is defective.	Replace C141 (0103-00-0949 sheet 7).
3. Offset gain and resolution problem.	DC offset circuit is malfunctioning.	Check for defective U27, U28, U29 and control logic (0103-00-0752 sheet 3). See table 6-20.

Table 6-7. Frequency Problems

Problem	Probable Cause	Solution
1. Output frequency locks up.	1. Frequency reference generator problem if 500 kHz signal is not sent to U110-13.	1. See table 6-23 and 0103-00-3021 (J2).
	2. Synthesizer phase lock loop is malfunctioning.	2. See table 6-24 and 0103-00-0949 sheet 5.

Table 6-7. Frequency Problems (Continued)

Problem	Probable Cause	Solution
2. Output frequency locks up to >50 MHz if >500 kHz is programmed.	1. Frequency at U109 <500 kHz.	1. Check for defective programmable ÷N counter and control logic.
	2. U109-12 <+3.9V. U109-4 does not pulse.	2. Check for defective U109.
	3. U111-3 is not +3.9V. U111-6 >0V.	3. Check for defective U111 and associated circuit.
	4. U114-6 voltage is different than U114-3.	4. Check for defective U114 and associated circuit.
3. No signal at FUNC OUT and SYNC OUT at all frequencies.	1. Power supply is malfunctioning.	1. Check ±15V and +5V supplies for correct voltage (Output/Power Supply schematic sheet 4). See tables 6-8, 6-9 and 6-10.
	2. Frequency reference circuit is malfunctioning if display is also not lit up.	2. Check frequency reference circuit (Output/Power Supply schematic). See table 6-23.
	3. VCO is not running if signal is not seen at U93-4 and U93-5 (Frequency Board schematic sheet 5).	3. Open the VCO shield cover and troubleshoot the VCO (see VCO schematic and table 6-30).
	4. No 100 MHz signal is seen at pin 1 of mixer Z1.	4. Check reference buffer amplifier or 100 MHz filter (table 6-27 and Frequency Board schematic sheet 7).
	5. No 100 MHz signal at pin 8 of Z1 is seen.	5. Check VCO and T1 (Frequency Board schematic sheet 7).
	6. Mixer/buffer amplifier is malfunctioning.	6. See table 6-27 and Frequency Board schematic sheet 7.

Table 6-8. +15V Regulator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 4)

Test Point	Observation
Q36-C	+18 to +23 Vdc, with 1 Vp-p signal.
Voltage across R295	+0.6 V.
CR39, zener voltage	6.2V ±5%.
U33-6	+3.6V.
Q38-C	+17V.
Q39-B	+15.4V.
Q39	Normally off, on if +15V supply is overloaded.
R307	+15V supply calibration.

Table 6-9. –15V Regulator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 4)

Test Point	Observation
Q43-C	– 18 to – 23 Vdc, with 100 mVp-p signal.
Voltage across R302	– 0.6V.
U34-3	0 Vdc.
U34-4	– 15V ± 20 mV normally referenced to and tracks with + 15V supply.
U34-6	– 3.6V.
Q41-C	– 17V.
Q44-B	– 15.5V.
Q39	Normally off, on if – 15V is overloaded

Table 6-10. +5V Regulator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 4)

Test Point	Observation
Q45-E	+ 7 to + 11 Vdc with 1 Vp-p signal.
U35-6, Q46-B	+ 0.6 Vdc.
U35-3, 2	+ 5.2 Vdc.
Voltage across R313, R314	+ 0.2 Vdc.
Q51, U36	+ 5V overvoltage protection.

Table 6-11. +5V Isolated Regulator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 4)

Test Point	Observation
VR1-1	+ 7 to + 11 Vdc with 800 mVac relative to programming ground ⏚.
VR1-3	+ 4.75 to + 5.25 Vdc from programming ground ⏚.

Table 6-12. +44V Isolated Regulator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 4)

Test Point	Observation
Q49-C	+50.5 to +51 Vdc.
Q50-C	+47 Vdc.
Q50-E	+11 Vdc.
CR48-C	+46 Vdc.

Table 6-13. Triangle Converter Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 2)

Test Condition: Set generator output to 1 kHz triangle waveform.

Test Point	Observation
Junction R84 and R85	1 kHz sine, 1.2 Vp-p.
U8-6	1 kHz triangle, 2.5 Vp-p.
U8-2, 3	0V ±40 mV.
U9-4	500 mVp-p, distorted sine.
U13-8	<0.8V (K3 on).
U13-6	+5V (K2 off).

Table 6-14. AM Circuit Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 2)

Test Condition: Set generator output to 1 kHz, AM sine.

Test Point	Observation
R53, Q9-B	1 kHz sine, 1.2 Vp-p.
U21-6, 3	+15V, FET switches on.
U21-11	−5V, FET switches off (+15V, FET switches on if frequency >500 kHz).
U17-12	−5V, negative supply from CR23 (A3).
U6-10	−0.7V.
U6-8	−0.7V.
U6-2, 3	−5 Vdc.
U6-5	−9.8 Vdc.
U6-1, 4	−4.3 Vdc.
U6-6	+5.2 Vdc swith 600 mVp-p sine.
U6-12	0 Vdc, into preamp summing junction.
Q11-E, Q12-E	6.7 Vdc with 600 mVp-p sine.
Q10-E	+0.7 Vdc.
Q9-E	+0.7 Vdc with 1.2 Vp-p sine.
Junction CR10 and R68	+8.8 Vdc.

Table 6-15. Sync and Square Wave Shaper Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 2)

Test Condition: Set generator output to 1 kHz triangle waveform.

Test Point	Observation
U7-7, 11, 2, 3	1 kHz square, ECL level. (ECL Level: High = 4.2V, Low = 3.5V.)
U21-14	+15V, FET switch on. −5V if square not selected.
Q14-C, Q15-C	0 to +4V square (no external load).
U7-12, 13	1 kHz square ECL, DC if square not selected.
Q16-C	2 Vp-p, 1 kHz square.
U21-13	110 mVp-p square.
Sync ϕ (near U7)	−5V if +1 Vp-p is selected. +4.5 V if −1 Vp-p is selected.

Table 6-16. Preamp Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 2)

Test Condition: Set generator output to 1 kHz sine waveform.

Test Point	Observation
Junction of R140 and R141	3.5 Vp-p sine, 0V offset (preamp output).
Junction of C59 and C62	0V, (amplifier summing junction).
U18-6	+15V, otherwise U18 defective.
U18-8	3.5 Vp-p sine, 0V offset.
U10-2	+1.2V.
Q18-B	+6.5V.
Q19-B	−6.5V.
R134	3.6 Vp-p sine, 0V offset for dc biasing.
U10, R143	For dc biasing.
C59, C62, C65, C66	Excess rolloff at high frequency if open.
C63, C64	Square wave peaking if open.

Table 6-17. Binary Attenuator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 2)

Test Condition: Set output amplitude to 5.12 Vp-p.

Test Point	Observation
U15-1	+15V.
U15-2, 14	−5V.
U16-2, 13, 1, 14	−5V.
U17-2, 13, 1, 14	−5V.
U18-1	3.5 Vp-p sine.
U18-16, 9	0V.
U19-8, 16, 1	0V.
U20-16, 1, 9, 8	0V.

NOTE

By using a similar procedure, set output amplitude to 2.56 Vp-p or 1.28 Vp-p. In this condition, only U18-16 or U18-9 will show a sine waveform. To check the lower order bits, set output amplitude to 1.27 Vp-p and check for a sine output from U19-8 to U20-8. The gate voltage at each transistor (SD5000) should be either −5V or +15V. If the voltages are not present, generally it indicates that the gate of the transistor is damaged and the transistor should be replaced. The SD5000 transistor is susceptible to static damage.

Table 6-18. Power Amplifier Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 3)

Test Condition: Set generator output to 5 Vp-p, 1 kHz sine, 0V offset into 50Ω load.

Test Point	Observation
FUNC OUT and R241	5 Vp-p sine and 0V offset.
Junction C85 and C88	0V, summing junction.
U29-6	0V, because offset is set to 0V.
Q22-B	+6 Vdc.
Q23-B	−6 Vdc.
Q25-B, Q28-E	1.7 Vp-p with +1.5 Vdc.
Q26-B, Q29-E	1.7 Vp-p with −1.5 Vdc.
Q24-B	+11 Vdc.
Q27-B	−11 Vdc.
Q30-E, Q32-E	+12.4 Vdc.
Q31-E, Q33-E	−12.4 Vdc.
U22-2	1.6 Vdc.
U22-3	+6 Vdc.
U22-10, 13	+8 Vdc.
C91 thru C94, C99, and R212	Amplitude flatness problem if defective.
C203, C204, C110, C97	Amplifier unstable if defective.
Most other capacitors	Slow rise/fall time if defective.

Table 6-19. Output Attenuator Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 3)

Amplitude Range	Output	Int Load	Relays (1 = On, 0 = Off) K10	K4	K5	K6	K7	K8	K9
			Pin No. of U31 (1 = High, 0 = Low) 16	2	12	15	5	6	9
1.00 to 10.00 mV	ON	IN	X	0	0	1	0	0	1
10.1 to 100.0 mV			X	0	0	1	0	1	0
100.1 to 1000 mV			X	0	1	0	0	1	0
1.01 to 10.00 V			X	1	0	0	1	0	1
10.02 to 20.00 V		OUT	X	1	0	0	1	0	0
50Ω to Gnd	OFF	IN	X	0	0	1	1	0	0
Open Circuit		OUT	X	0	0	1	0	0	0
	Front Output		0	X	X	X	X	X	X
	Rear Output		1	X	X	X	X	X	X

Table 6-20. DC Offset Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 3)

Test Condition: Set output amplitude to 1.01 Vp-p.

Programmed DC Offset	U27 Pin At High State	U28-6 Voltage	U29-6 Voltage
+2.56V	13	+3.8	+3.8
+1.28V	12	+2	+2
+0.64V	11	+1	+1
+0.48V	10, 9	+0.7	+0.7
+0.155V	8, 7, 6, 5, 4	+0.2	+0.2
0V	None	0	0
−2.56V	12, 13	+3.8	−3.8

Table 6-21. Function Control Logic Troubleshooting Information

Waveform	Frequency	Output/Power Supply Board Schematic Sheet 2							Frequency Board Schematic Sheet 1		Sheet 2				
		Pin No. of U11							Pin No. of U5						
		12	2	15	5	9	6								
		Pin No. of U21													
		11	6	14				3	9	2					
		Relay (1 = On 0 = Off)									Pin No. of U36 (ECL Levels: High = 4.2V, Low = 3.5V)				
					K1	K2	K3		K1		5	2	3	14	9
Sine	>500 kHz	0	0	0	0	0	1	0	0	1	1	0	DC	⎍	⎍
	≤500 kHz	0	0	0	1	0	0	0	0	0	0	1	⎍	DC	⎍
Triangle	≤500 kHz	0	0	0	0	1	0	0	0	0	0	1	⎍	DC	⎍
Square	>500 kHz	0	0	1	0	0	0	0	0	1	1	0	DC	⎍	⎍
	≤500 kHz	0	0	1	0	0	0	0	0	0	0	1	⎍	DC	⎍
Ramp	≤20 kHz	0	0	0	0	1	0	0	1	0	0	1	⎍	DC	⎍
DC		0	0	0	0	0	0	0	0	0	0	1	⎍	0	⎍
AM (∿)	>500 kHz	1	0	0	0	0	0	1	0	1	1	0	DC	⎍	⎍
	≤500 kHz	0	1	0	0	0	0	1	0	0	0	1	⎍	DC	⎍

Table 6-22. Low Frequency Mixer Troubleshooting Information (Ref: Output/Power Supply Schematic Sheet 1)

Test Condition: Program the instrument to reset condition.

Test Point	Observation
E6 at R1	1 MHz TTL.
Q2-E	1 MHz, 2 Vp-p.
U1-6	1 MHz sine, 1.2 Vp-p.
U1-1, 8	1 MHz sine, 1 to 1.5 Vp-p, +4V Offset.
U2-6, U3-6	1 MHz sine, 1 to 1.5 Vp-p.
E8 at CR3	1.001 MHz TTL.
Q3-C, Q4-C	+10V to −0.5V square.
Junction of R32 and R33	−7.5 Vdc.
Q5-S	1.2 Vp-p signal.
U5-3	1 kHz, 500 mVp-p sine.
Q8-E	1 kHz, 1.2 Vp-p sine.
Ramp 1 (near Q7)	<0.8V if sine or triangle are selected. >2V if ramp is selected.

Table 6-23. Frequency Reference Troubleshooting Information (Ref: Reference Board Schematic)

NOTE: Use X10 probe with short ground clip.

Test Point	Observation
A. Without EXT REF signal.	
Q2-C	10 MHz TTL level.
Q1-S	10 MHz, 2 Vp-p.
U7-8	>3V if no EXT REF signal.
U8-9	1 MHz TTL.
U6-9	500 kHz TTL.
E3 at C38	10 MHz 1.5 Vp-p sine.
U9-1	10 MHz ≈10 ns positive pulse.
Q4-S	50 MHz ≈800 mVp-p.
U4-6, U4-7	50 MHz ECL. (ECL Level: High = 4.2V, Low = 3.5)
U4-3	100 MHz ECL.
Q5-S	100 MHz ≈250 mVp-p.
Q6-C	100 MHz ≈2 Vp-p.
B. Apply 10 MHz signal to EXT REF IN.	
U5-11	10 MHz TTL.
U6-5	1 MHz 30 ns pulse.
U1-4	1 MHz 930 ns pulse.
U1-5	Low if REF locked. Pulses if REF not locked.
U7-8	<0.8V if EXT REF signal present.
U3-2	1.5V
U3-6	1 to +12V.
U2-13, 2	Mostly high with 930 ns pulse when phase locked.

Table 6-24. Synthesizer Phase Lock Loop Troubleshooting Information (Ref: Frequency Board Schematic Sheet 5)

Test Condition: Program output frequency to 10.0 MHz	
Test Point	**Observation**
U110-13	500 kHz ECL reference signal. (ECL Level: High = 4.2V, Low = 3.5V)
U93-4, 5, 6, 15	110 MHz ECL.
U94-2, 3	55 MHz ECL.
U95-14	500 kHz, 10 ns negative pulses.
U97-11	Pulses, but always < +3.9V.
U94-15, 14	500 kHz, 10 ns pulses.
U95-6,11,13, U96-5,6,12,13	> +3.5V frequency programming input.
U95-5,12 U96-11	< +3.5V frequency programming input.
U98-14, U99-3, 6	500 kHz, 290 ns pulse width.
Q10-C	500 kHz, TTL, 290 ns pulse width.
U109-4	< +3.9V with pulse <10 ns.
U109-12	> +3.9V, with pulse >10 ns.
U111-3, 2	+3.9V.
U111-6	> +2V but < +10V.
U114-6	> +2V but < +10V.
U103-6	>0V but < +14V.

Table 6-25. Delay Generator Troubleshooting Information (Ref: Frequency Board Schematic Sheet 6)

Test Condition: Program generator frequency to 10.0 MHz.

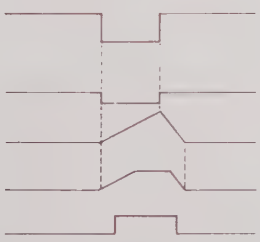
Test Point	Observation
Q24-B, Q25-B	500 kHz, 290 ns complementary pulses.
Q27-B, E	500 kHz pulse, see the following timing diagram.
U112-2, 3	−0.8V, amplifier summing junction.
U112-6	0V.
Q20-E	+6.7V.
Q23-E	−6.7V.
Q26-E	Triggered ramp waveform.
U113-10, 13	500 kHz pulses.
U113-16	−8V.
U113-2, 6	500 kHz, 0.7V pulses, +4.5V offset.
U102-6	+8.5 Vdc.
U102-9	0 to −1V. (Also see U102-9 under second test condition.)
U107-2	0 Vdc.
U107-6	0 to +5V.
Q18-D	−8.7V offset. (Also see Q18-D under second test condition.)
U104-2, 3	+8.5V.
Q15-E	+3V approximately.
Q19-E	−9V.
Q16-S	−5V approximately.
Q27-E C105 Q26-E U113-4 U113-10	

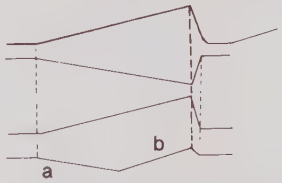
Table 6-25. Delay Generator Troubleshooting Information (Continued)

Test Condition: Program generator to 1.005 MHz	
Test Point	**Observation**
U102-9	600 mV ramp signal.
Q18-D	– 8.7 Vdc approximately.

* Use Tektronics x 10 scope probe, P6075A, and a short ground lead to examine this signal. Synchronize scope to TP1 (anode side at CR21) Ref: Frequency Board Schematic sheet 5, coordinates A5.

Table 6-26. High Frequency Compensation Circuit Troubleshooting Information (Ref: Frequency Board Schematic Sheet 6)

Test Conditions: Sweep Start Frequency 500 kHz.
Sweep Stop Frequency 50 MHz.
Sweep Mode Continuous.
Sweep Time .02 sec

Test Point	Observation
SWP OUT U105-10, 8 U105-14 Q13-D	

NOTE: The slope of segments **a** *and* **b** *of Q13-D are adjustable independently by adjusting the pots R144 and R151.*

Table 6-27. Mixer and Buffer Amplifier Troubleshooting Information (Ref: Frequency Board Schematic Sheet 7)

Test Conditions: Program output frequency to 1 MHz.

Test Point	Observation*
U115-5, 2, 3	100 MHz, ECL.
U115-14, 15	100 MHz, ECL.
Q31-E	+7.5V.
Q33-C	100 MHz, 400 mVp-p.
J17-3 (On VCO Board)	101 MHz, 6 Vp-p.
Junction of L6 and C138	1 MHz, 40-50 mVp-p.
Q34-E, Q35-E, Q36-E	+11V.
Q39-C	1 MHz 150 mVp-p, with +10 Vdc.
Q40-C	1 MHz 450 mVp-p, with +10 Vdc.
Q41-C	1 MHz 1.2 Vp-p, with +5 Vdc.
U117-6	0 Vdc (sine, 100 times the output frequency if 1 kHz or lower frequency is programmed).
U116-6	+12.2 Vdc approximately.
Q37-C, Q38-C	1 MHz, 0.7 Vp-p with 3.9 Vdc.
U37-2, 14, 15	1 MHz, ECL.
Q29-C	1 MHz, TTL.

*Use Tektronics X10 scope probe, P6075A, and a short ground lead to examine these high frequency signals.

Table 6-28. Divide-by-100 Counters Troubleshooting Information (Ref: Frequency Board Schematic Sheets 1 and 2)

Test Point	Observation
Test Condition: Program generator frequency to 200 kHz, continuous.	
U28-4, 5, 2	100 MHz, ECL. (ECL Level: High = 4.2V, Low = 3.5V.)
U28-9, 6, U29-2	> +3.9V.
U28-7, U32-2	< +3.9V.
U29-15, U30-3, 14	20 MHz, ECL, unsymmetrical.
U25-2, 14, U24-2, 3	4 MHz, ECL, unsymmetrical.
U118-2, U18-10, 8	4 MHz, TTL.
U1-5, 6, 8, 9	1 MHz, TTL, symmetrical.
U31-7, 3	120 MHz, ECL.
U32-15, U33-3, 14	24 MHz, ECL, unsymmetrical.
U26-2, 14, U24-14, 15	4.8 MHz, ECL, unsymmetrical.
U118-7, U3-3	4.8 MHz, TTL.
U3-5, 6, 8, 9	1.2 MHz, TTL, symmetrical.
U4-5	1.2 MHz, TTL.
U18-1, 2	1 MHz.
U18-3	2 MHz.
U35-4	2 MHz, adjustable pulse width by R17.
U34-5	1 MHz, TTL, symmetrical.
Test Conditions: Generator frequency 200 kHz, trigger mode without triggering signal.	
U28-9, 6, U29-2	< +3.9V.
U28-7, U32-2	> +3.9V.
U29, U30, U25, U18	Same as above.
U31-7, 3	100 MHz, ECL. (ECL Level: High 4.2V, Low = 3.5V.)
U32-15, U33-3, 14	20 MHz, ECL.
U26-2, 14, U24-14, 15	4 MHz, ECL.
U118-7, U3-3	4 MHz, TTL.
U3-5, 6, 8, 9	1 MHz, TTL.
U4-5	1 MHz.

Table 6-29. Trigger Slope and Trigger Source Control Logic Troubleshooting Information (Ref: Frequency Board Schematic Sheet 1)

Test Conditions	Test Point	Observation
1. Trigger Slope Positive	U5-16	L
	U7-2	L
	U7-3	Invert of U9-13
2. Trigger Slope Negative	U5-16	H
	U7-2	H
	U7-3	Same phase as U9-13
3. External Trigger Source	U5-19	L
	U16-9	L
	U16-8	H
	U16-6	H
	U16-12	H
	U8-12	Trigger Signal
4. Internal Trigger Source	U5-19	H
	U16-9	H
	U16-8	L
	U8-12	H
	U16-6	Internal trigger signal
	U16-12	Internal trigger signal

NOTE: See also Figure 4-12 for trigger mode timing diagram.

Table 6-30. VCO Troubleshooting Information (Ref: VCO Board Schematic)

Test Condition: Program 10 MHz sine wave. Use high impedance probe with short ground lead.

Problem	Probable Cause	Solution
1. No waveform at P17-2, 3 (VCO output)	Problem may be in output buffer amplifier or voltage controlled oscillator.	Check VCO pins at P16 and P17 for proper connection.
2. No sine wave at Q2-C.	Q2 may be defective if sine wave is not present.	Check for 2 Vp-p sine wave signal and −7 Vdc offset at Q2-B, Check L5 for open coil.
3. No sine wave at Q2-B.	Problem may be in voltage controlled oscillator.	Check for 4 Vp-p sine wave at the junction of R5 and C10 and −8 Vdc at Q1-G, Q1 may be bad otherwise check for shorted varactor diodes CR1 through CR6, check L1, L2, L4.
4. VCO frequency unstable.	Problem may be caused by L2.	Check L2 for 11 turn ratio and that it is held down as close to ground as possible.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted in the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, next higher assembly and unit serial number.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

The number etched into a PC board is the board part number. The assembly (PC board and components on the board) part number is stamped on the board.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0168
Display/Logic Schematic	0103-00-1378
Display/Logic Assembly	1100-00-1378
Display/Logic Parts List	1100-00-1378
Reference Schematic	0103-00-3021
Reference Assembly	1100-00-3021
Reference Piggyback Assembly	0101-00-3021
Reference Parts List	1100-00-3021
VCO Schematic	0103-00-2642
VCO Assembly	1208-00-2642
VCO Parts List	1208-00-2642
Frequency Generator Schematic	1104-00-3397
Frequency Generator Assembly	1101-00-3397
Frequency Generator Parts List	1100-00-3397
Output/Power Supply Schematic	0103-00-0752
Output/Power Supply Assembly	1100-00-0752
Output/Power Supply Parts List	1100-00-0752
Rear Panel Schematic	0103-00-0814
Rear Panel Assembly	0102-00-0814
Rear Panel Parts List	1101-00-0814
GPIB Decoder Assembly and Parts List	0101-00-0865

DRAWING	DRAWING NUMBER
Front Panel Assembly	0102-00-0892
Front Panel Parts List	1101-00-0892
Chassis Assembly	0102-00-0812
Chassis Parts List	1101-00-0812
Stored Settings Installation	0002-00-0169
Stored Settings Schematic	0103-00-0822
Stored Settings Assembly	1100-00-0822
Stored Settings Parts List	1100-00-0822

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REV	ECN	BY	DATE	APP
A	#2725	[illegible]	[illegible]	
B	#3012	[illegible]	[illegible]	[illegible]
C	ECN 4204	[illegible]	3.8.89	[illegible]
D	ECN #4444	[illegible]	3-28-89	[illegible]

REAR PANEL ASSY (P/N 1101-00-0814) (A3)

J28 CORCOM — L P R S

POWER SWITCH — 4 3 2

TRIG IN J24 | MARKER OUT J25 | Ø MOD IN J27 | AM IN J26

W1 W2 W3 W4 W23

XFMR

W24 GND, +5V UNREGULATED; W25 ISO 44VAC; W26 ISO 44VAC; ISO 5VAC; ISO 5VAC; GND; 5VAC; 15VAC

FUNC OUT J20 | SYNC OUT J21 | REF IN J22 | REF OUT J23

W5 W6 W7 W8

GPIB ADDRESS SELECTOR SWITCH 5 4 3 2 1

J18 P18

J19

E44 E45 E32 E31 E35 E40 E41 E13 E12 E22 E23 P4 J4 E1 E5 E3 E4

FREQUENCY GENERATOR BD (P/N 1100-00-0949) (A6)

J9 500 KHz–50 MHz W12 → E10 E11

J10 TRIGGER W11 → E14 E15

J11 1 MHz W10 → E6 E7

J12 1–1.5 MHz IN W9 → E8 E9

E39 +5V-1 W20 → J37

E18 E19 E16 E17

REFERENCE BOARD (P/N 1100-00-3021) (P/N 1100-00-3022 FOR 002 OPTION) (A5)

STORED SETTINGS BOARD (OPTION) (P/N 1100-00-0942) (A9)

J40 W30 J38

A15 GND A14 A5 A13 GND A12 ISS TEST A11 GND A10 GND A9 GND A8 GND DB7 GND DB6 GND DB5 +5V DB4 GND DB3 +5V DB2 GND DB1 30MHZ DB0 +NL R/W

OUTPUT/POWER SUPPLY BOARD (P/N 1100-00-0752) (A4)

J13 P7 J7

BD0 W26 BD1 BD2 BD3 BD4 BD5 BD6 BD7 ATTN OFST L11 OFST L0 AMPL WAVE N.C. LOCKSENSE +5V GND GND N.C. N.C.

E28 → LOCKSENSE W19 ← E2

VCO BOARD (P/N 1208-00-0751) (A7)

J17 P17 P16 J16

P14 J14 +15V W21 P8 J8

GND −15V +5V +5V +5V GND +5V ISO ISO GND +44V ISO

E25 GND W22 −15V-2 +5V-2 +5V-1 P1 J1

E26 E24 E27 E29 E30 J6

E38 E37 E43 E42 500 KHz W13 120 MHz IN W14 J2 J3

J39 E33 E34 J15

W5 4MHz WHT BLK SERO W29 +5V TEST T TEST SERT ISO GND ISO GND +5V ISO +5V ISO +5V ISO ISO GND ISO GND ISO GND +44V ISO GND GND GND 4MHz CLK

W27 D701 D705 D702 D706 D703 D707 D704 D708 EOT +5V LOGIC GND +5VAC LOGIC GND +5VAC LOGIC GND +5VAC

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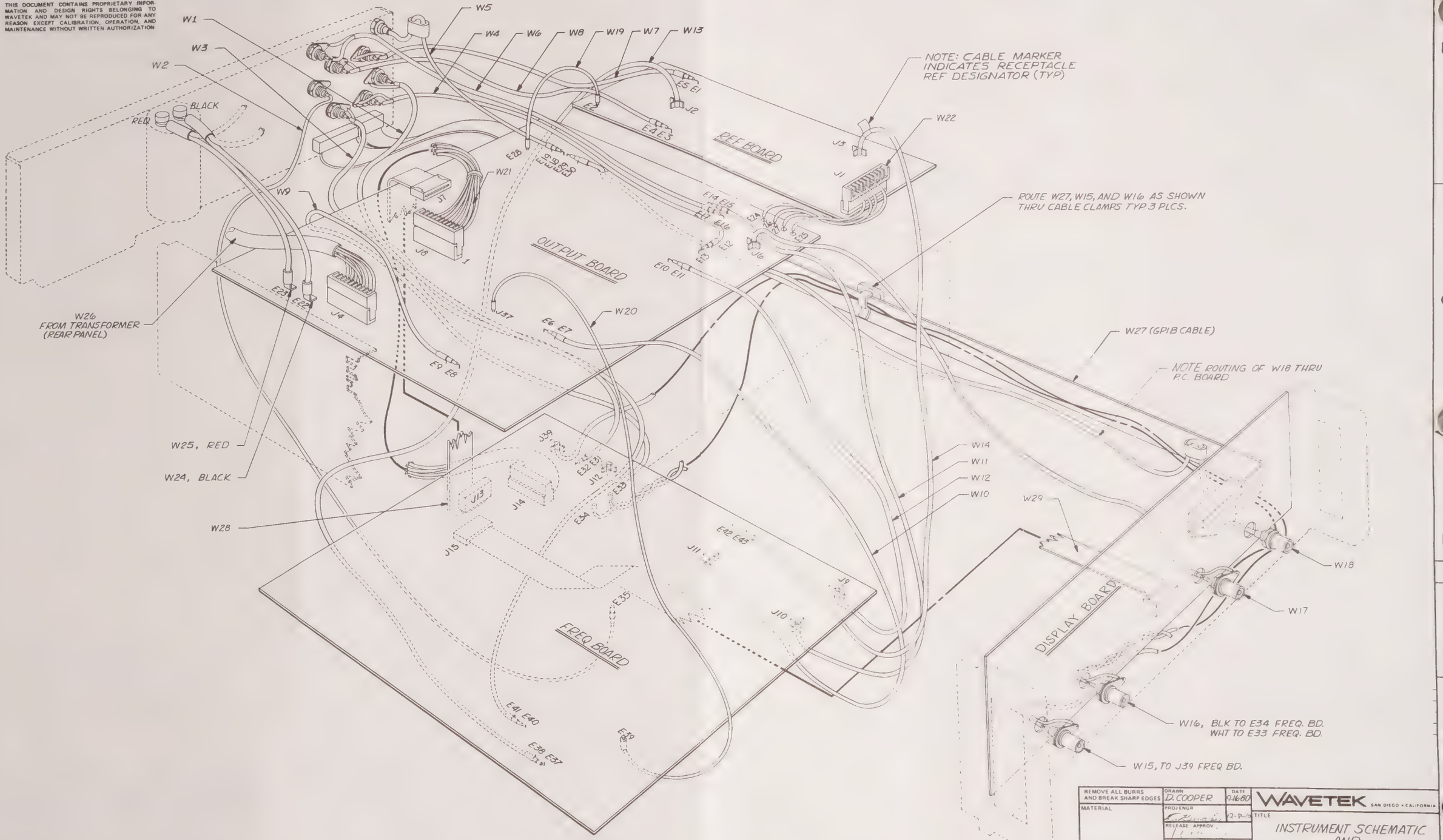
REV	ECN	BY	DATE	APP.



1. THIS DRAWING IS INTENDED TO SHOW THE CABLE INSTALLATION AND APPROX. CABLE ROUTING.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9.1680	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		INSTRUMENT SCHEMATIC AND CABLE ROUTING
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 178	DWG NO 0004-00-0168 REV F
		CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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µP #1 CONTROL CIRCUIT

NO.	E.N.	BY	DATE	APP.
C	7002 7171	RD	3/1/94	
B	8159			
D	7007			

TEST OPTION

C5 27pf SM

+5I

VCC VCC STBY

XTAL1

EXTAL2

Y1

4MHZ CLK (B1)

4 TURNS (BRN)

5 TURNS (WHT)

T1

C3 .1/50V

C4 .1/50V

R13 499

R11 150K

R12 49.9K

Q1 2N3903

R5 1K

C6 27 pf SM

CR7 FD777

MODE SELECTION OPTION

C49 .1x01

R14 3.65K

CR8

MR (307,304)

R7 100K SIP

R6 4.02K

C1 220 pf 500V SM

U16 1/2 393

R8 3.01K

R9 1K

CR9

R10 100K

U17 1/6 LS04

SYR (C1)

U25 1/4 CD4093BE

RESET

CR1 CR2 CR3

R15 R16 10K (1)

R17

C50 6.8/50V

1/4 LS08

BLANK (2B4,2C5)

DSP (2D4)

P20 INED6

P21 OLVL

P22 XCLK

EXT UART CLK (B1)

E1 E2 E3

XCLK (D1)

R23 2.49K

REC (C1,2A4)

P23(REC)

U23 140.10

U26 1/4 LS08

RESET

DIG+5V

+5V

R18 182

U24 6N136

R19 100K

R3 100K

U26 4093BE

U25

R55 2.49K

R4 1K

C2 .1/50V

U27 1/4 LS00

TPQ

SERO (A1)

SERI (B1)

1/6 LS04

U17

P24(XMIT)

XMIT (C1)

VSS

1/4 LS00

U27

(D5)E

(D5)R/W

WRP/

E (C1,B4,B5,2C7,3D7,3D4)

1/4 LS08 U26

TP3

BE (D1,A4,2B3)

TP8

TP5,6,7

R24 10K

R25 10K

R/W

AS

R/W (C1,B4,B6,3C4,3C7)

AS (C1)

74LS373

U6

P30 AD0
P31 AD1
P32 AD2
P33 AD3
P34 AD4
P35 AD5
P36 AD6
P37 AD7

HOOK-UP IS TYPICAL TO THAT OF U18, U19 AND U20 (B6,B7)

D0 D1 D2 D3 D4 D5 D6 D7 → Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7

OE

P40 ADR8 (C1,B4-B8)
P41 ADR9 (C1, B5-B8)
P42 ADR10 (C1, B6-B8)
P43 ADR11 (C1,B8,A6,A7)
P44 ADR12 (C1,A8)
P45 ADR13 (C1,A6,A7)
P46 ADR14 (C1,A4,C5)
P47 ADR15 (C1,A4,C5)

P10 KOUT0 (2A6)
P11 KOUT1 (2A6)
P12 KOUT2 (2A6)
P13 KOUT3 (2A5)
P14 KIN0
P15 KIN1 (2B8)
P16 KIN2
P17 BEEP (2A3)

NMI (C1)

TP4

F 26 3.32K

R27 3.32K

IRQ

U1-40 (3B7,3B4)

GPIB BUS TRANSCEIVER INTERFACE (SEE SHT 3 OF 3)

TEST CONN.

J32-

	1,2	+5I
	3	AD7
	5	AD6
(D5)	7	AD5
	8	AD4
	9	AD1
	11	AD3
(C6)	12	XCLK
	13	AD2
(D5)	14	BE
	15	AD0
	16	R/W
(C5)	17	ADR8
(C5)	18	NMI
(C5)	19	ADR14
(D5)	20	AS
	21	ADR15
(C5)	22	ADR10
	24	ADR9
	26	ADR11
(B6)	27	XMIT
(C5)	28	ADR12
(C6)	29	REC
(C5)	30	ADR13
(D5)	31	E
(C7)	32	SYR
	33,34	ISO GND

J30-

(D7)	1	4MHZ CLK
	2	DG
	3	DG
	4	DG
	5	+44V ISO
	6	ISO GND
	7	ISO GND
	8	ISO GND
	9	+5 ISO
	10	+5 ISO
	11	+5 ISO
	12	+5 ISO
	13	ISO GND
	14	ISO GND
(B6)	15	SER I
	16	N/C
(C7)	17	EXT UART CLK
	18	N/C
	19	+5V
(B7)	20	SERO

PROGRAM / MEMORY

(IC U19 NOT LOADED)

U19 U20

ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7 ADR8 ADR9 ADR10 ADR11 ADR12

(D4) A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12

O0 O1 O2 O3 O4 O5 O6 O7

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

(C5) CE OE

(A3) ROM1/ (A3) ROM2/ ADR13 ADR13

+5I

U21 6116

ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7 ADR8 ADR9 ADR10

I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

RAM/ CS OE

(D5) E R/W

(C5) ADR14 ADR15 CE1 CE2 U5

R35 R38 1K(4)

GPIB/ (3C7,3C4)

SEG CK/ (2C6)

U4

(D5) BE

R39 1K R40 1K R42 1K(3)

ROM1/ (B7)

ROM2/ (B7)

NC

RAM/ A5

9. ⏚ = DIGITAL GND.
8. ⏚ = ISO GND.
7. SIPS
   R7=100K
   R30=10K
   R43=1.5K
   R47=10K
6. REF DES NOT USED: R1,R2, R31 - R34, R41
5. ALL CAPACITORS ARE IN µf.
4. ALL RESISTORS ARE IN OHMS.
3. ALL DIODES ARE FD6666.
2. + = MOUNTED ON SOCKET.
1. PARTIAL REFERENCE DESIGNATORS SHOWN, PREFIX WITH ASSEMBLY REF DES (A8).

NOTE UNLESS OTHERWISE SPECIFIED

FB1 ISO+5V → +5I

C10 1000/16V

C11,18,21,22 THRU 43, 45,47 .1/50V

FB2 +5V → DIG+5V

C12 100/16V

C13 .1/50V

FB3 +44V ISO → +44V

C14 47/50V

C15,17,19,20 .1/50V

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RANGE	DATE 5/1/94	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR Flinks	7/14/94	TITLE: SCHEMATIC: DISPLAY AND KEYBOARD (µP-GPIB) (A8)
FINISH WAVETEK PROCESS	RELEASE APPROV Ed Ide		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0103-00-1378 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1894

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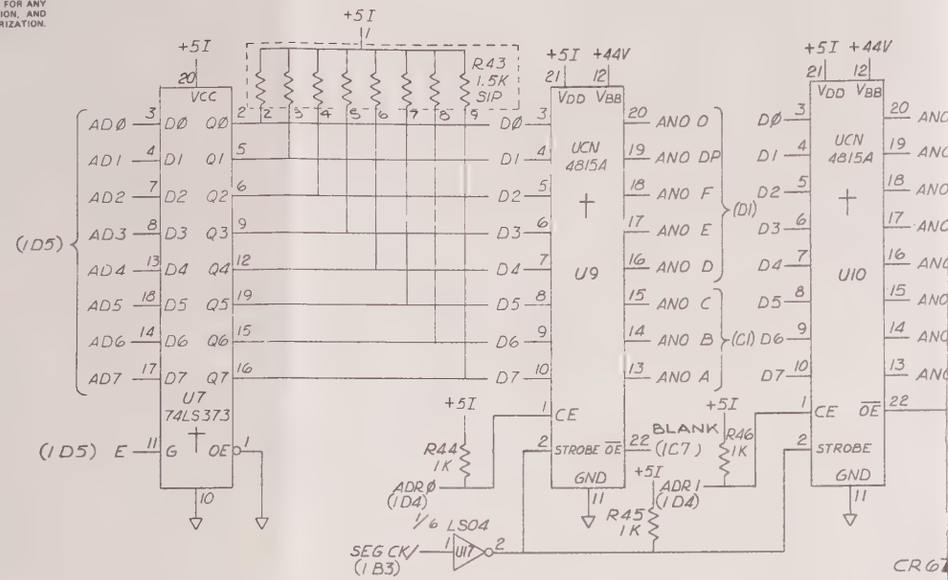
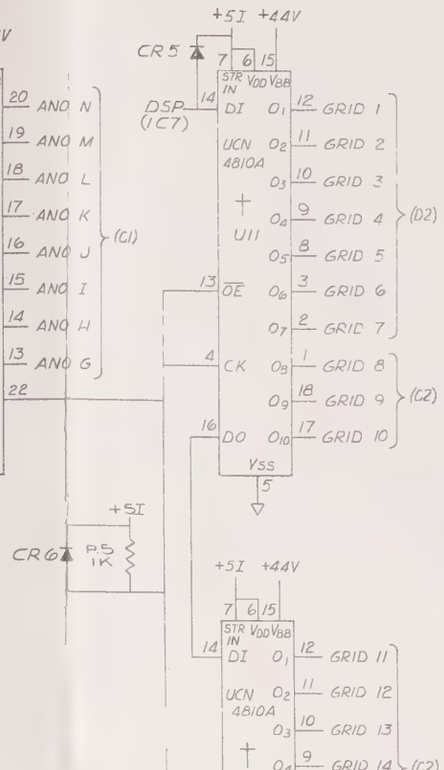
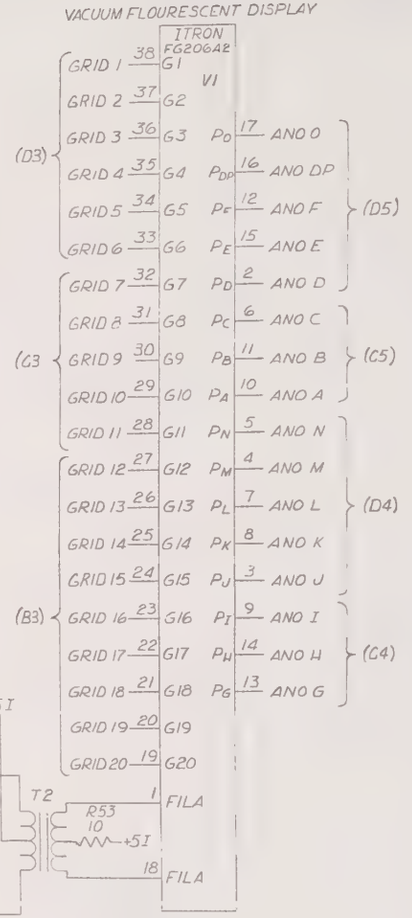
REV	ECN	BY	DATE	APP

DISPLAY LOGIC

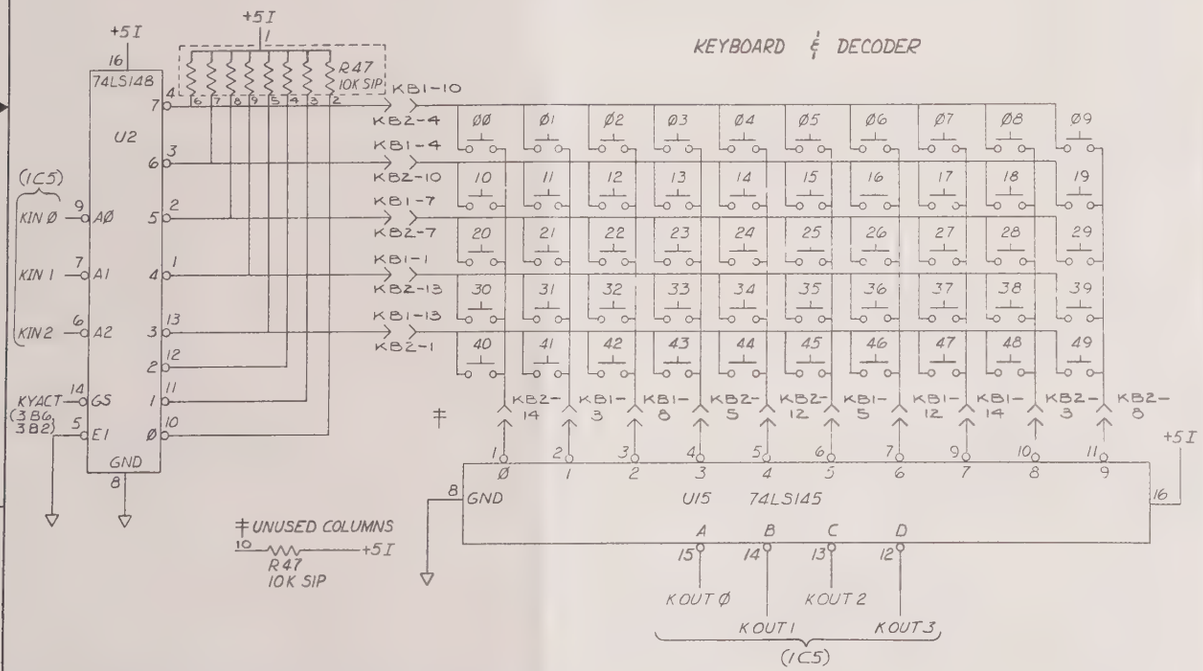



+5I +44V
CR5
DSP (IC7)
STR IN VDD VBB
DI O1 O2 O3 O4 O5 O6 O7 O8 O9 O10
UCN 4810A
U11
OE CK DO Vss
GRID 1 GRID 2 GRID 3 GRID 4 GRID 5 GRID 6 GRID 7 GRID 8 GRID 9 GRID 10
(D2)
CR6
R5 1K
U8
GRID 11 GRID 12 GRID 13 GRID 14 GRID 15 GRID 16 GRID 17 GRID 18 GRID 19 GRID 20
(C2)
(B2)
BLANK (IC7)

VACUUM FLOURESCENT DISPLAY

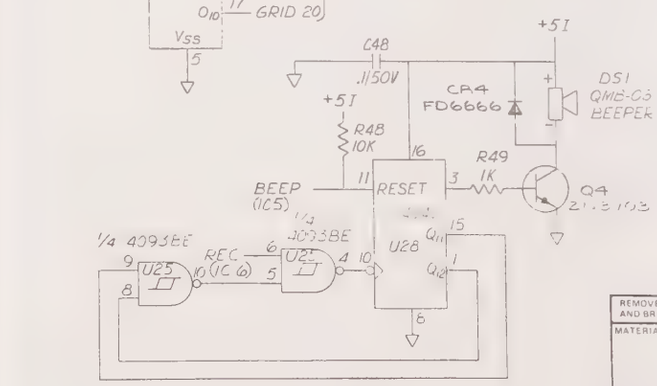

ITRON FG206AR
VI
GRID 1 GRID 2 GRID 3 GRID 4 GRID 5 GRID 6 GRID 7 GRID 8 GRID 9 GRID 10 GRID 11 GRID 12 GRID 13 GRID 14 GRID 15 GRID 16 GRID 17 GRID 18 GRID 19 GRID 20
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20
(D3)
(G3)
(B3)
PO PDP PF PE PD PC PB PA PN PM PL PK PJ PI PH PG
ANO 0 ANO DP ANO F ANO E ANO D ANO C ANO B ANO A ANO N ANO M ANO L ANO K ANO J ANO I ANO H ANO G
(D5)
(C5)
(D4)
(C4)
FILA FILA

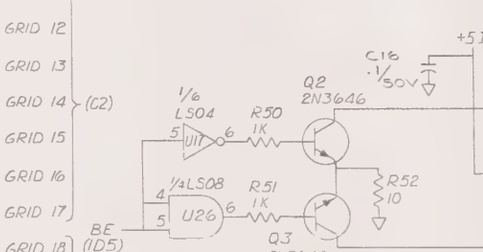
KEYBOARD & DECODER


+5I
R47 10K SIP
U2 74LS148
(IC5)
KIN 0 KIN 1 KIN 2
A0 A1 A2
KYACT (3B6 3B2)
GS EI
GND
KB1-10 KB2-4 KB1-4 KB2-10 KB1-7 KB2-7 KB1-1 KB2-13 KB1-13 KB2-1
Ø0 Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8 Ø9
KB2-14 KB1-3 KB1-8 KB2-5 KB2-12 KB1-5 KB1-12 KB1-14 KB2-3 KB2-8
‡ UNUSED COLUMNS
U15 74LS145
A B C D
KOUT Ø KOUT 1 KOUT 2 KOUT 3
(IC5)

‡ UNUSED COLUMNS
KB1-2,6,9,11
KB2-2,6,9,11

NOTE UNLESS OTHERWISE SPECIFIED





REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RANGE	DATE 5/3/84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROTENGR [illegible]	7/26/84	TITLE: SCHEMATIC: DISPLAY AND KEYBOARD (A8)
FINISH WAVETEK PROCESS	RELEASE, APPROV [illegible]		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0103-00-1378 REV D
	SCALE	CODE IDENT 23338	SHEET 2 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3984

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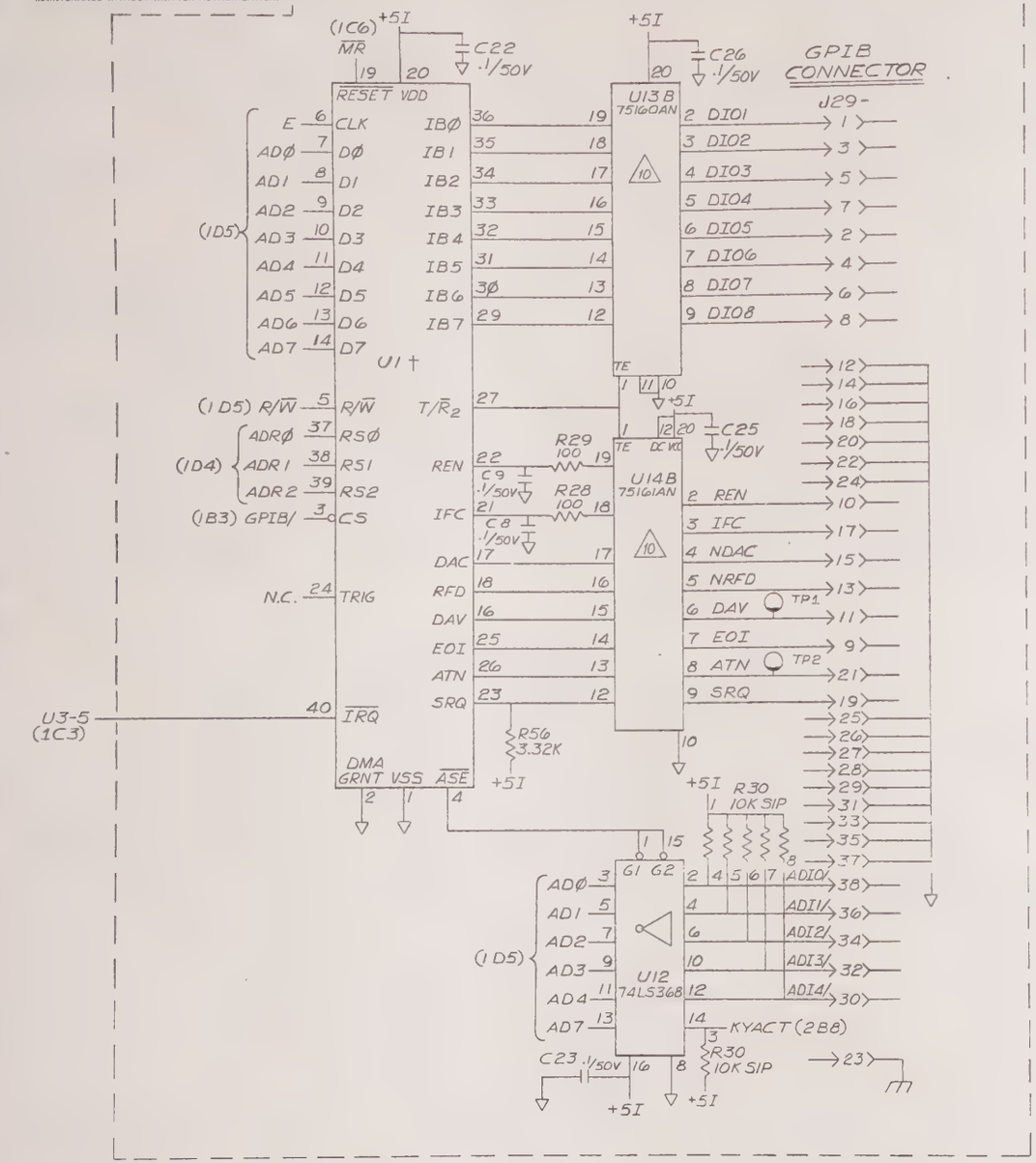
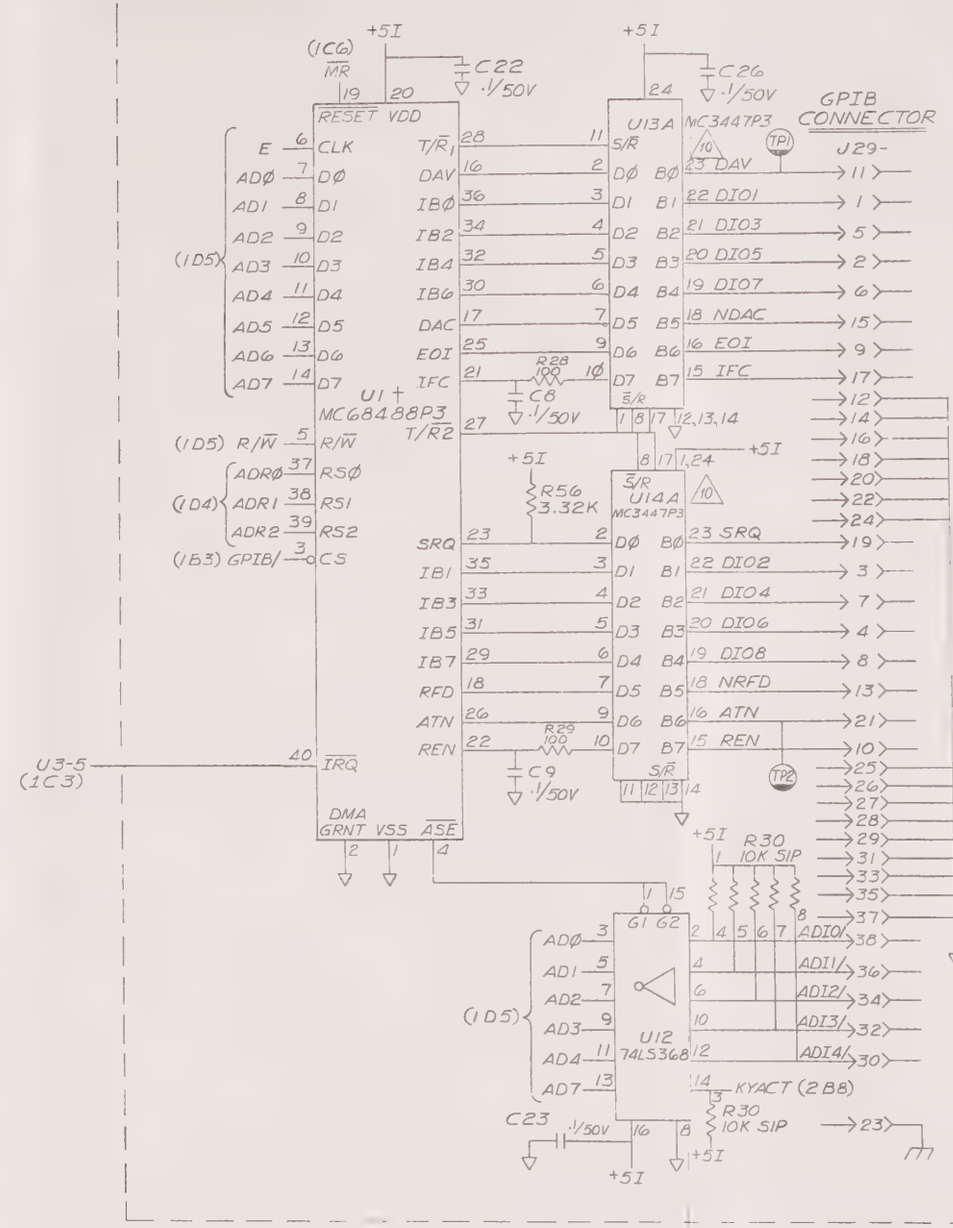
REV	ECN	BY	DATE	APP

"T.I." BUS TRANSCEIVER CONFIGURATION



"MOTOROLA" BUS TRANSCEIVER CONFIGURATION



10 U13A AND U14A IS USED ONLY IF MOTOROLA'S MC 3447P3 IS USED IN LOADING OF BOARDS.-OR- U13B AND U14B IS USED ONLY IF T.I.'S 75160 AN/ 75161 AN IS USED IN LOADING OF BOARDS.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RANGE	DATE 5/3/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR	7/14/84	TITLE: SCHEMATIC: DISPLAY AND KEYBOARD (μP-GPIB)(A8)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0103-00-1378 REV D
	SCALE	CODE IDENT 23338	SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3084

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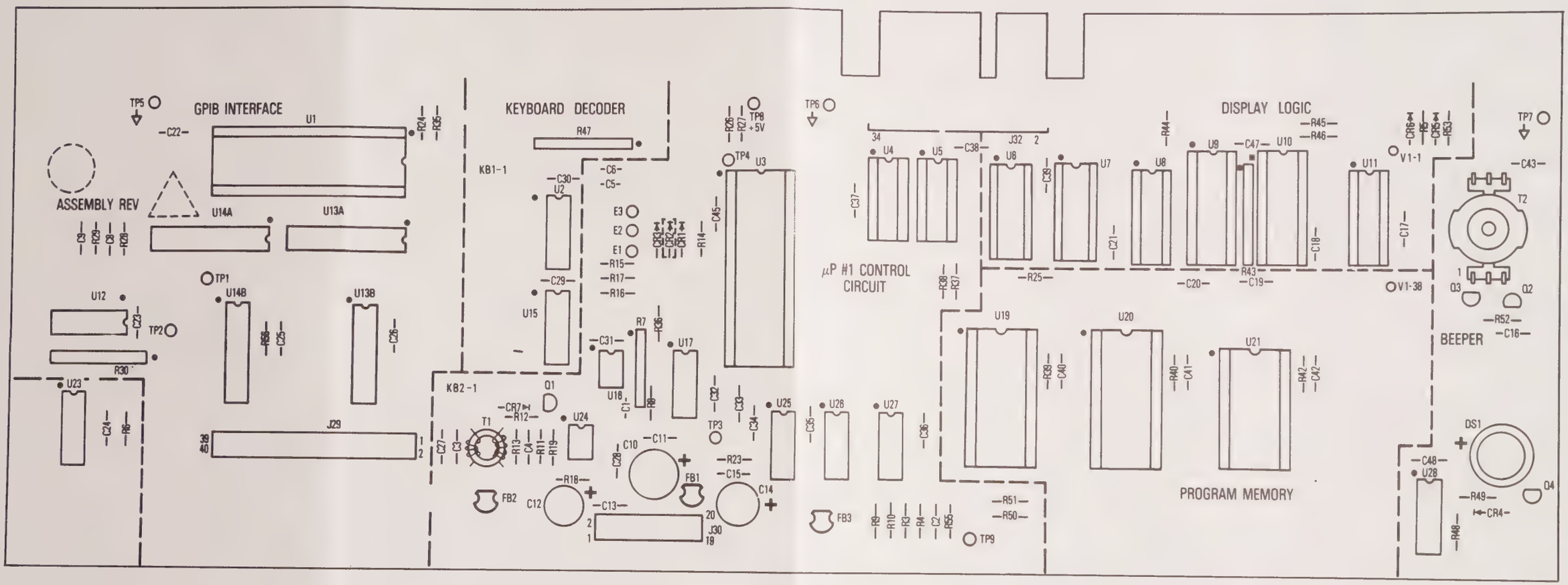

MADE FROM 0100-00-1378-3D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA DISPLAY/LOGIC
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-1378 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFOR MATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DISPLAY LOGIC BD	0101-00-1378	WVTK	0101-00-1378	1
NONE	SCHEMATIC, DISPLAY LOGIC BD	0103-00-1378	WVTK	0103-00-1378	1
T2	TRANSFORMER, DISPLAY	178-0033	WVTK	1204-00-0033	1
T1	TRANSFORMER	1204-00-0037	WVTK	1204-00-0037	1
NONE	SPK ASSY, KEYBOARD	178/270-0939	WVTK	1206-00-0939	2
C49	CAP, CER, .001MF, 1KV	DD-102 LONG LEAD	CRL	1500-01-0201	1
C11 C13 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C4 C40 C41 C42 C43 C45 C47 C48 C8 C9	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	39
C1	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
C12	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	1
C10	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	CRE SERIES 1000/16	CAPAR	1500-31-0211	1
C14	CAP, ELECT, 47MF, 50V RADIAL LEAD, SP .20	ULB1J470M	NICH	1500-34-7003	1

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R28 R29	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R35 R36 R37 R38 R39 R4 R40 R42 R44 R45 R46 R49 R5 R50 R51 R57 R9	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	17
R15 R16 R17 R24 R25 R48	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	6
R10 R19 R3	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	3
R52 R53	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	2
R11	RES, MF, 1/8W, 1%, 150K	RN55D-1503F	TRW	4701-03-1503	1
R18	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R23 R55	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R8	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R26 R27 R56	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	3
R14	RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R6	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R13	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R12	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R30 R47	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	2

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	BIMOS				
U21	RAM 2K X 8, CMOS STATIC	CXK5816PN-12L	SONY	8000-61-1600	1
U3	MICROPROCESSOR, 8BIT	MC6803L	MOT	8000-68-0300	1
U27	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U17	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	1
U26	GATE AND, QUAD 2-INP, TTL	74LS08	TI	8000-74-0810	1
U23 U28	COUNTER, 12 BIT NIN, CMOS	14040	RCA	8001-40-4000	2
U1	ADPT, GPIB INTERFACE	MC6848BP	MOT	8006-84-8800	1
U15	CDDR/DRV, BCD-DEC, TTL	74LS145	SIG	8007-41-4510	1
U2	ENCODER, 8-3 OCTAL, TTL	74LS148	TI	8007-41-4810	1
U12	HEX INVERTER, 4-BIT + 2-BIT	74LS368	TI	8007-43-6810	1
U6 U7	LATCH, OCTAL TRANSPAR W/3 STATE	74LS373	MOT	8007-43-7310	2
U5	IC, PROGRAMMED V1.0, REF 8008-21-2601	8600-00-0204	WVTK	8600-00-0204	1

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C50	CAP, TANT, 6.8MF, 50V	TAP6.8M50	ITT	1500-76-8503	1
NONE	PCB, DISPLAY LOGIC BD	1700-00-1378	WVTK	1700-00-1378	1
NONE	SKT, IC, 16PIN	DILB16P-108T	BURND	2100-03-0028	2
NONE	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	1
NONE	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	2
NONE	SKT, IC, 22 PIN	DILB22P-108T	BURND	2100-03-0035	2
NONE	SOCKET, 18 PIN	DILB18P-108T	BURND	2100-03-0050	2
NONE	SOCKET, 20 PIN	DILB20P-108T	BURND	2100-03-0051	2
NONE	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	2
NONE	SOCKET, 8 PIN	DILB08P-108T	BURND	2100-03-0063	1
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	9
J30	CONN, HEADER, 20 PIN	929836-01-10	AP	2100-05-0042	1
J29	CONN, HEADER	929836-02-20	A/P	2100-05-0048	1
V1	DISPLAY, FLOUR.	FG206A2	ITRON	2400-03-0009	1
NONE	BEEPER	GMB-06	STMIC	3000-00-0085	1
FB1 FB2 FB3	BALUN CORE	2873000902	FARIT	3100-00-0002	3

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R43	RES NETWORK 1.5K 2% 10PIN SIP BUSS	785-1R1.5K	BECK	4770-00-0010	1
R7	RES NETWORK 100K 2% 8PIN SIP ISOL	764-3-R100K	BECK	4770-00-0032	1
CR7	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	1
CR1 CR3 CR4 CR5 CR6 CR8 CR9	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	7
Q2 Q3	TRANS, NPN, -TO-92	2N3646	NSC	4901-03-6460	2
Q1 Q4	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3903	NSC	4901-03-9030	2
U16	COMPARATOR, LOW POWER LOW OFFSET VOLTAGE DUAL	LM393N	NSC	7000-03-9300	1
U24	OPTO CPLR, FAST	6N136	SPECT	7100-00-0001	1
U13 U14	BUS XCVR, BIDIR, O, TTL	MC3447P3	MOT	8000-34-4700	2
U25	GATE, NAND, S/TRG GUA, CMOS	CD4093BE	RCA	8000-40-9300	1
U11 U8	DRIVER, 10 BIT SI, BIMOS	TL4810AN	TI	8000-48-1000	2
U10 U9	DRIVER, LTCH/SORC,	UCN5815A	SPRAG	8000-48-1500	2

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U20	IC, PROGRAMMED V2.4 REF 8002-71-2800, MODEL 178	8600-00-0362	WVTK	8600-00-0362	1
U4	IC, PROGRAMMED V1.0 REF 8008-21-2601	8600-00-0363	WVTK	8600-00-0363	1

WAVETEK PARTS LIST | TITLE: DISPLAY, LOGIC BD | ASSEMBLY NO. 1100-00-1378 | REV C | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, DISPLAY/LOGIC
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-1378 REV C
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

B SHOP GRAPHICS ACCUPRESS REORDER NO. X7106

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REV	ECN	BY	DATE	APP
A	ERO # 3321	GMG	8-5-16	

FROM OUTPUT BD J1-
E27 5
E24 7
E26 9
E25 10
N/C 8
N/C 6
N/C 4
N/C 3
N/C 2
N/C 1

+5.2V-1 FB1
+15V-1 FB2
-15V-1 FB3
+5.2V-2 FB4
+15V-2 FB5
-15V-2 FB6
E9 TO E17 (2B6)
+5.2V-3
+15V-3
-15V-3

C1 .1
C2 .1
C3 .1
C4 100/16V
C5 100/16V
C6 100/16V
C7 1000/16V
C8 100/16V
C9 100/16V
C62 22/15V
C63 .1
C66 .1

EXT. REFERENCE PHASE LOCK

TP1
R1 2.49K
C64 .1
U7 7416
U2 MC4044
FROM E13 (2C3) E11
E6
TO E18 & E19 (2B6)
E7
R55 301
C10 .01
R5 15K
R54 2.49K
R2 15K
CR1
CR3
CR2
CR4
R3 19.1K
R4 19.1K
C11 .01
C12 .01
C13 .1
R6 20.5K
R7 301K
R8 30.1K
R9 301K
C14 .1μF POLY
C15 .1
C16 .1
U3 LF356
R10 499
C17 .01
R11 10K
CR5
R12 499K
R13 10K
R14 24.9K
C18 .1
CR7 MV2209
C19 .1
C20 *
R15 1K
R16 10K
CR8
CR9
Y1 10MHz

10MHz REFERENCE OSCILLATOR

R17 499
C24 .01
Q1 2N5485
C22 82pf SM
C23 82pf SM
R18 4.99K
C25 100pf
R19 2.49K
R20 24.9K
R21 1.5K
Q2 2N3646

E12 TO E15 (2B4)

TO E14 (2B4) E10

10 MHz EXT REF IN FROM REAR PANEL J22

E1
C27 330pf
R22 1K
R23 100
E5
U5 NE529
CR10
CR11
R24 100
C29 .1
-15V-3

70ns PULSE SET

R25 10K
R26 10K, 1%
C30 150pf SM
U6 74LS74
U1 74123
TP2
R27 1K
+5.2V-3

R28 49.9K
C31 .01
CR14 HP2811
E2 LOCK SENSE
C32 .01
C61 47pf SM

U9 74S02
U8 74LS290 ÷10
1,7,13
R30 249
C33 47pf
C34 30pf SM
CR12 FD777

R31 51.1
C35 47pf
L1 5.6uh
C36 68pf SM
C37 91pf SM
C38 220pf SM
E3 10 MHz REF OUT TO REAR PANEL J23
E4
C65 .1
R32 100
Q3 2N3646
J2 500 KHz REF OUT TO FREQ BOARD E37, E76
R33 21.5
R34 301
C39 100pf

10 MHz

X5 MULTIPLIER

R35 100
C42 .01
L4 130nH
Q4 2N5485
L3 129.7nH
CR13 FD777
C40 56pf SM
C41 7-35pf
C45 7-35pf
C46 82pf SM
C97 270pf SM
R38 499
C43 22pf
R36 499
R37 100
C44 .01
R39 301
R40 301
C48 .01
R41 499
R42 499
R43 301
R44 301
R45 301
C49 100pf
C50 100pf
TP3
10116

DOUBLER

C51 22/15V
C52 100pf SM
L2 .12μH
R46 249

100MHz BUFFER

L5 62nH
Q5 2N5485
C53 3.5-13pf
C54 43pf SM NOM
R48 2.49K
R47 100
C56 .01
L6 130nH
C52 68pf SM (NOM)
C59 27pf SM NOM
J3 100 MHz REF OUT TO FREQ BOARD E42, E43
R49 4.99K
C57 100pf
R50 10K
Q6 A-400
FB
R51 750
R52 15
C61 33pf
C60 .001
C55 .01
R53 100

5. *NOM VALUE CALLED OUT ON P/L.
4. L3 THRU L6 ARE PRINTED CIRCUIT BOARD INDUCTORS
3. PARTIAL REFERENCE DESIGNATORS SHOWN, PREFIX WITH ASSEMBLY REF DES (A5)
2. CR1 — 6, 8 — 11 ARE FD6666
1. ALL RESISTORS ARE IN OHMS

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S CHERMACK
PROJECTOR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CA & IOWA

TITLE: SCHEMATIC REFERENCE BOARD (A5)

MODEL NO 178 | DWG NO 0103-00-3021 | REV A
CODE IDENT 23338 | SHEET 1 OF 2

0103-00-9280

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3000

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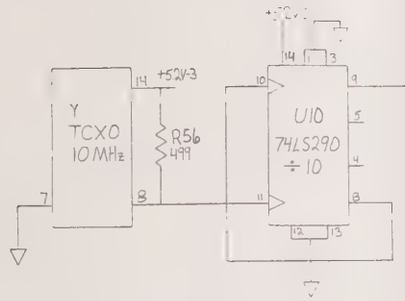
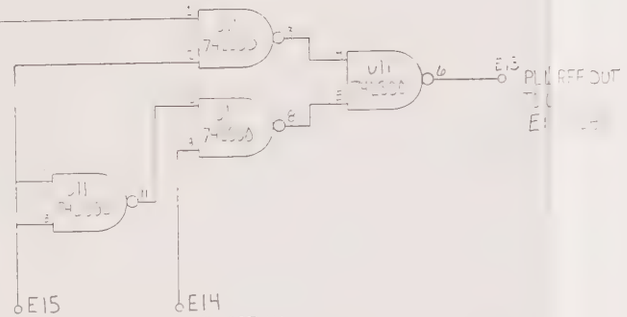
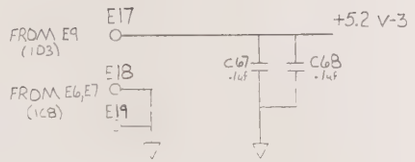
REV	ECN	BY	DATE	APP







NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN G.GOOD	DATE 8-4-87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	4-2-87	TITLE
	RELEASE APPROV		SCHEMATIC REFERENCE BOARD (45)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO. 178-00-3021 REV A
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

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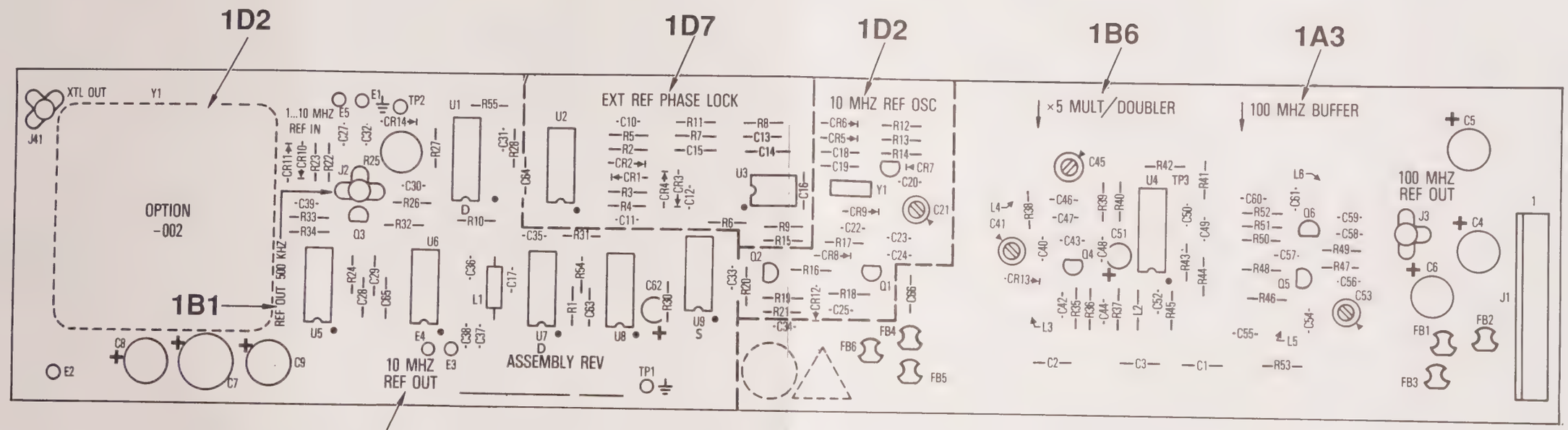

REFERENCE KEY: 2D3

SCHEMATIC SHEET NO.
VERTICAL COORDINATE
HORIZONTAL COORDINATE

DRAWING MADE FROM
0100-00-0928-3 REV A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PCA REFERENCE
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 178 · DWG NO 1100-00-3021 · REV
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

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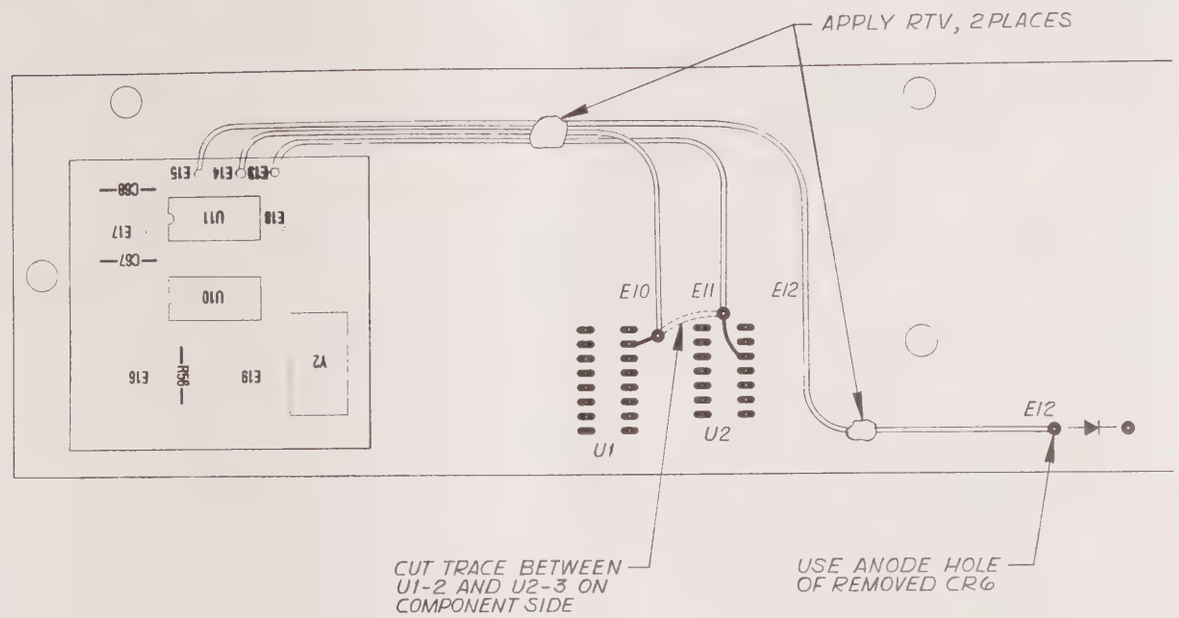
REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: ASSEMBLY REFERENCE BOARD

MODEL NO	DWG NO	REV
178	0101-00-3021	A

CODE IDENT 23338

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, REFERENCE BD	0101-00-3021	WVTK	0101-00-3021	1
NONE	ASSY DWG, CABLE KIT	0102-00-0873	WVTK	0102-00-0873	1
NONE	SCHEMATIC, REFERENCE BD	0103-00-3021	WVTK	0103-00-3021	1
NONE	ASSY, WIRE 178-0928	1207-00-2792	WVTK	1207-00-2792	1
NONE	ASSY, WIRE 178-0928	1207-00-2793	WVTK	1207-00-2793	1
NONE	SHIELD PARTITION	178-0171	WVTK	1400-01-0171	2
NONE	SHIELD PARTITION	178-0181	WVTK	1400-01-0181	2
NONE	COVER	178-0223	WVTK	1400-01-0223	1
NONE	SHIELD PARTITION	178-1281	WVTK	1400-01-1281	1
NONE	CORNER POST(X) REF: 3200-02-0004	178-1311	WVTK	1400-01-1311	4
C25 C39 C49 C50 C57	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	5
C60	CAP, CER, .001UF, 1KV	DD-102	CRL	1500-01-0211	1
C10 C11 C12 C17 C24 C31 C32 C42 C44 C48 C55 C56	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	12
C1 C13 C15 C16 C18 C19 C2 C28 C29 C3 C63 C64 C65 C66 C67 C68	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	16

WAVETEK PARTS LIST | TITLE: PCA, REFERENCE BD. | ASSEMBLY NO. 1100-00-3021 | REV B | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C43	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
C61	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C27	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C35	CAP, CER, 47PF, 1KV	DD-470	CRL	1500-04-7011	1
C52	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	1
C30	CAP, MICA, 150PF, 500V	DM15-151J	ARCO	1500-11-5100	1
C38	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
C20T	CAP, MICA, 24PF, 500V, 1%	CM05CD240D03	CDE	1500-12-4006	1
C59T	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	1
C47	CAP, MICA, 270PF, 500V	DM15-271J	ARCO	1500-12-7100	1
C34	CAP, MICA, 30PF, 500V, RADIAL	DM15-300J	ARCO	1500-13-0000	1
C54T	CAP, MICA, 43PF, 500V	DM15-430J	ARCO	1500-14-3000	1
C33 C69	CAP, MICA, 47PF, 500V	DM15-470J	ARCO	1500-14-7000	2
C40	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	1
C36 C38T	CAP, MICA, 68PF, 500V	DM15-680J	ARCO	1500-16-8000	2

WAVETEK PARTS LIST | TITLE: PCA, REFERENCE BD. | ASSEMBLY NO. 1100-00-3021 | REV B | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C22 C23 C46	CAP, MICA, 82PF, 500V	DM15-820J	ARCO	1500-18-2000	3
C37	CAP, MICA, 91PF, 500V	DM15-910J	ARCO	1500-19-1000	1
C4 C5 C6 C8 C9	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	5
C7	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE 1000/16	NIC	1500-31-0211	1
C14	CAP, MYLAR, .1MF, 100V	225P10491WD3	BPRAD	1500-41-0444	1
C53	CAP, VAR, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	1
C41 C45	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	2
C51 C62	CAP, TANT, 22MF, 20V	202A2002226M3	MATSO	1500-72-2621	2
NONE	REFERENCE BOARD	178-0928	WVTK	1700-00-0928	1
NONE	PCB OSCILLATOR BD (REF. 3021)	1700-00-2999	WVTK	1700-00-2999	1
L1	CHOKE, 5.6MH	1537-30	DELVN	1800-00-0015	1
L2	INDUCTOR, .12MICRO H	1025-96	DELVN	1800-00-0019	1
J1	CONN, HEADER	1-640386-0	AMP	2100-02-0079	1
J2 J3	CONN, COAX SOCKET	226287-2	AMP	2100-03-0038	2
J2A J3A	SPRING SOCKET	50935-1	AMP	2100-03-0039	2

WAVETEK PARTS LIST | TITLE: PCA, REFERENCE BD. | ASSEMBLY NO. 1100-00-3021 | REV B | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	PIN, MALE	60809-2	AMP	2100-05-0020	1
TP1 TP2	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	2
E16 E17 E18 E19	CONN PIN, MALE (UOM-EA PIN)	CA-S36SP-100-230-B30	CA	2100-05-0034	4
Y1	CRYSTAL, 10MHZ	2300-99-0007	SAVOY	2300-99-0007	1
Y2	OSCILLATOR, TEMP COMPENSATED 10MHZ XTAL, 14	7400B10MHZ0 030LEAD DI	MONIT	2300-99-0026	1
NONE	WASHER, FLT #6, .187 OD, .141 ID, .047THK, NYLON	2515	SMITH	2800-26-0002	6
NONE	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	1
FB1 FB2 FB3 FB4 FB5 FB6	BALUN CORE	2873000902	FARIT	3100-00-0002	6
R25	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	1
R23 R24 R32 R35 R37 R47 R53	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	7
R15 R22 R27	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	3
R11 R13 R16 R26 R50	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	5
R21	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
R2 R5	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2

WAVETEK PARTS LIST | TITLE: PCA, REFERENCE BD. | ASSEMBLY NO. 1100-00-3021 | REV B | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R52	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	1
R3 R4	RES, MF, 1/8W, 1%, 19.1K	RN55D-1912F	TRW	4701-03-1912	2
R6	RES, MF, 1/8W, 1%, 20.5K	RN55D-2052F	TRW	4701-03-2052	1
R33	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	1
R30 R46	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R1 R19 R48 R54	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	4
R14 R20	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	2
R34 R39 R40 R43 R44 R45 R55	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	7
R8	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R7 R9	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	2
R10 R17 R38 R41 R42 R56	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	6
R12 R18 R36 R49	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	4
R28	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R31	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R51	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
CR7	DIODE, GEN PUR TUNING	MV2109	MOT	4803-02-2109	1
CR12 CR13	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	2
CR1 CR10 CR11 CR2 CR3 CR4 CR5 CR8 CR9	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	9
CR14	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	1
Q2 Q3	TRANS, NPN, -TO-92	MPS3646	MOT	4901-03-6460	2
Q1 Q4 Q5	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-03-4850	3
Q6	TRANS	A-400	AMPRX	4902-00-4000	1
U3	OP-AMP	LF356N	NSC	7000-03-5600	1
U5	IC	NE529N	SIG	7000-05-2900	1
U11	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U9	GATE, NOR, QUAD 2-INPUT	74S02	SIG	8000-74-0201	1
U7	INVERTER BUFRS/DRVRS, HEX, W/OC HIGH VOLT O/P	7416	SIG	8000-74-1600	1
U6	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	1
U4	RCVR, TRI LINE, ECL	MC10116P	MOT	8001-01-1600	1
U1	MULT VIBRTRS, DL RETRIGGERABLE MONOS W/CLEAR	74123	TI	8007-41-2300	1
U10 U8	COUNTER, BCD, TTL	74LS290	TI	8007-42-9010	2
U2	IC	MC4044P	MOT	8100-40-4400	1

WAVETEK PARTS LIST | TITLE: PCA, REFERENCE BD | ASSEMBLY NO. 1100-00-3021 | REV B | PAGE 5

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, REFERENCE BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 1100-00-3021 / REV B
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27089

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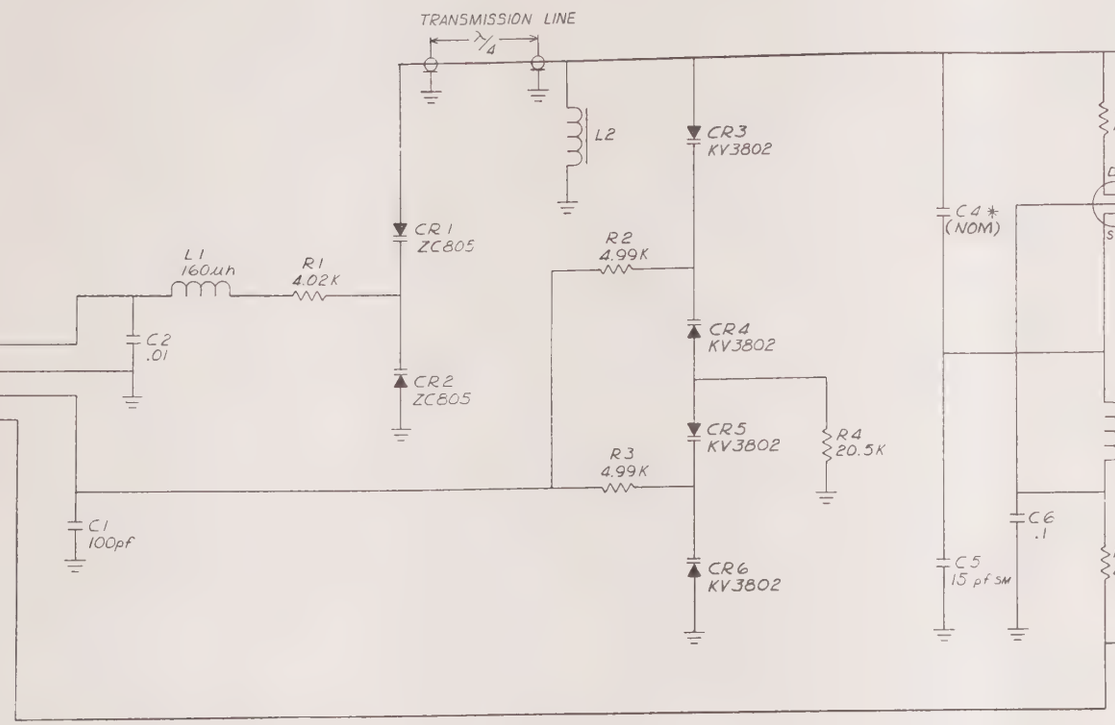
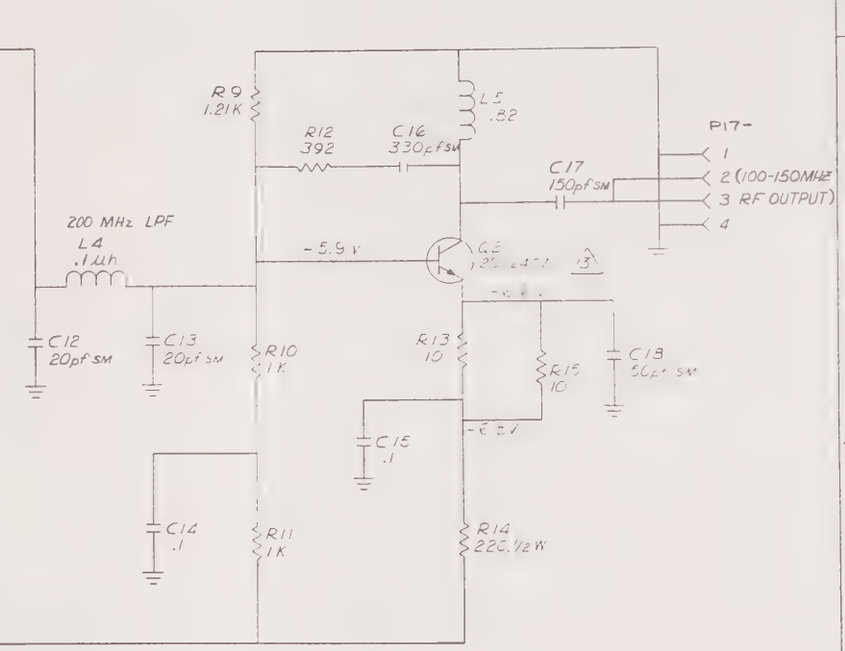
REV	ECN	BY	DATE
A	RELEASE #007965	SC	[illegible]

TRANSMISSION LINE
VOLTAGE CONTROLLED OSCILLATOR



OUTPUT BUFFER AMP



4. * = NOMINAL VALUE CALLED OUT ON PARTS LIST.
3. Q2 BOTTOM VIEW- B E C
2. ALL RESISTORS ARE IN OHMS.
1. PARTIAL REFERENCE DESIGNATORS SHOWN. PREFIX WITH ASSEMBLY REF DES (A7)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S CHERMACK	DATE 5-20-87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: VCO BOARD (A7)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1 XX : 030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 0103-00-2642 / REV A
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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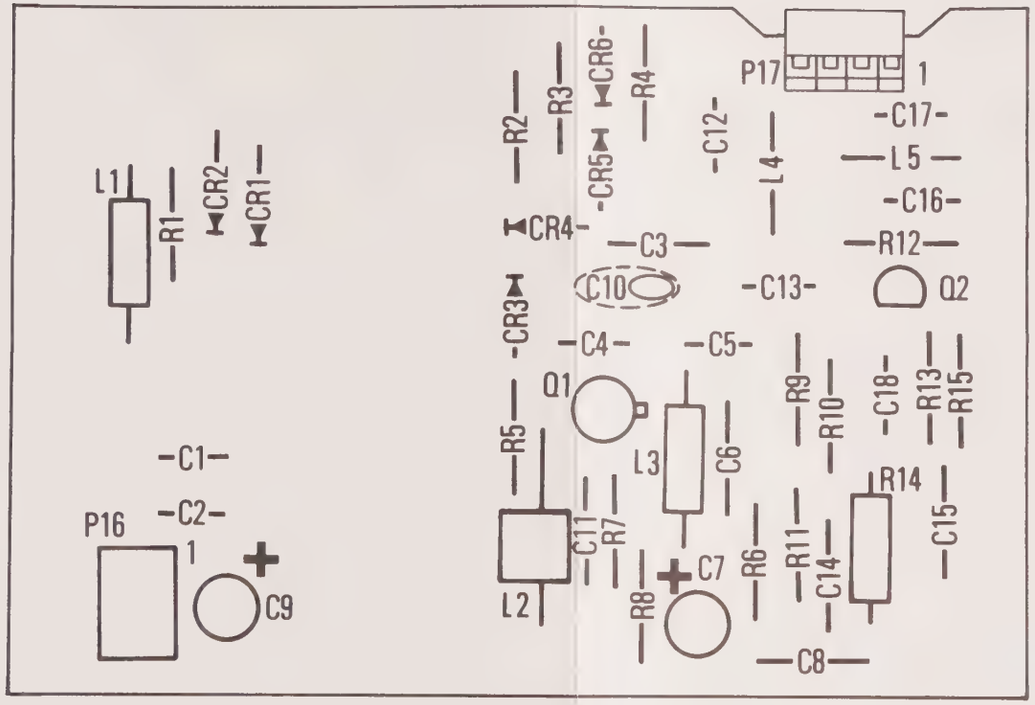

MADE FROM 0100-00-2642-3B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA VCO
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178
	SCALE		DWG NO 1208-00-2642 REV
			CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, VCO BOARD	0101-00-2642	WVTK	0101-00-2642	1
NONE	SCHEMATIC, VCO BOARD	0103-00-2642	WVTK	0103-00-2642	1
L2	COIL, VCO	178-0040	WVTK	1204-00-0040	1
C1	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	1
C2	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C11 C14 C15 C6 C8	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	5
C10	CAP CER MON 2.7PF 50V	CCD2R7DNPO	ARCO	1500-02-7505	1
C4 C5	CAP, MICA, 15PF, 500V	DM15-150J	ARCO	1500-11-5000	2
C17	CAP, MICA, 150PF, 500V	DM15-151J	ARCO	1500-11-5100	1
C12 C13	CAP, MICA, 20PF, 500V, RADIAL	DM15-200J	ARCO	1500-12-0000	2
C16	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	1
C18	CAP, MICA, 50PF, 500V	DM15-500J	ARCO	1500-15-0000	1
C7 C9	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	2
NONE	PCB, VCO BD REF: SPEC 0008-00-0455 REV C	1700-00-2642	WVTK	1700-00-2642	1
L1 L3	CHOKE, 160MH	1537-86	DLVAN	1800-00-0016	2

WAVETEK PARTS LIST | TITLE: ASSY VCO BD | ASSEMBLY NO. 1208-00-2642 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
L4	INDUCTOR, .1 MICRO H	1025-94	DELVN	1800-00-0020	1
L5	INDUCTOR, 82MICRO H	1025-18	DLVAN	1800-00-0024	1
P16 P17	CONN, .100 CTR, 4 POS, GLD PLT, BOT ENT, PC MT	22-17-2042	MOLEX	2100-02-0065	2
R14	RES, C, 1/2W, 5%, 220	RC-1/2-221J	STKPL	4700-25-2200	1
R10 R11	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R13 R15 R5	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	3
R9	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R6	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R4	RES, MF, 1/8W, 1%, 20.5K	RN55D-2052F	TRW	4701-03-2052	1
R12	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R1	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R2 R3 R7 R8	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	4
CR1 CR2	DIODE	ZC-805	MSI	4803-02-0805	2
CR3 CR4 CR5 CR6	DIODE	KV3802	KSW	4803-02-3802	4
Q1	DMOS FET, N-CHAN, ENHANCE MODE, LATERAL	SD-202DC/SR	SPI	4902-00-2020	1
Q2	TRANS	NE41632E-1-D	CEL	4902-02-1320	1

WAVETEK PARTS LIST | TITLE: ASSY VCO BD | ASSEMBLY NO. 1208-00-2642 | REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST VCO
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1208-00-2642 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
A	ECO # 90-343	MS	6/3/90	

TRIGGER CONTROL LOGIC

+5V
R1 10K
MAN TRIG (3C5)
CR1
U9 LS132
R4 332
J51 TRIG IN (REAR)
J39 TRIG IN (FRONT)
R5 1.21K
CR2
J39A
U7 LS86
C3 .001
R7 249
GO SWEEP (D5)(3B2)
SWEEP (D5)(3A4)
R8 249
C5 100pf
U5-16 (A8)
÷4 (REF)
R3 249
C2 100
(C7)(3A4) GO SWEEP
SWEEP (C7)(3A4)
R34, R35 RST SW (2 B2)
U8 LS10
U16 LS10
U5-9 (A8)
U5-12 (A8)
R6 249
C4 100
U15 LS02
TRIG SWP
U48-2 (3 B4)
U5-15 (A8)
C1 .1
R2 2.49K
U14 LS74
HI FREQ SQU/ (A 5)
CONT BURST
U43-27(3C3)
U2-6(B6)
GO BURST
GO BURST/
U64-9(3 D3)
U2-3(B5)
U6 74LS132
U14-1(D2)
R9 249
C6 10pf
SYNC
U43-28(3C3), R46(2A6)
POWER SUPPLY CONN.
U14- P14-
1 +15V
2 GND
3 -15V
4,5,6 +5V
7 GND
8 +5V ISO
9 ISO GND
10 +44V ISO

4MHz CLK (2 C1)
U18 LS86
÷4 (VARIABLE FREQ)
NC
R13 2.49K
U1 LS74
C7 .1
U18-1 (A2)
U18-2 (A2)
U10 LS02
U11 LS109
C9 .01
U14-8 (C1)
U2 7401
U14-9 (C1)
R15 499
C14 *
U11-7 (A4)
CR3
R10 499
R11 316
C8 .0022
U13 74S10
U22-13(A4)
U23-8(A5)
U22 LS20
U2-8 (A7)
U20 74S 74
HI FREQ SQU/ (A 5)
R12 316
CR4
U20-4 (A6)
C10 220pf
R14 100
C12 .001pf
C13 68pf
U12 LS02
4-6 MHz VAR FREQ (2 B1)
C11 .01
U3 LS74
R47 (2 A5)
C209 100pf
U2 7401
K1 (7 A2)
U4 LS 151
R18 100
U12
1-1.5 MHz
J12A
TO 3D1
U5 LS273
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
U46-10 (3C1)
U8-10 (D5)
U15-11 (D4)
U7-12,2 (C 8)
U16-9 (D7)
U19-13 (B4)
R20 2.49K
U11-6 (A4)
÷100 (SYNC)
U22-1 (C4)
U27 74S02
U21 74S74
U20 74S74
U5-2 (B1)
SQU (7 D1)
HI FREQ SQU/ (B3)
U20-13 (B3)
R21 2.49K
C16 .1
U11 LS109
U22-4 (B4)
U22-2 (B4)
U18 LS86
U5-9 (A7)
U19 74LS00
U2-8 (A7)
U10-9 (C5)
U27-2(C4)
1 MHz DELAY
U10-2(C6)
U10-3(C6)
U35 LS123
C15 56pf SM
R16 *
C17 .01
R17 TRIG BASELINE ADJ 10K
+15V-2
U34 LS74
R19 100
U11 (1 MHz)
J11A

5. SIP VALUES ARE:
R22 R112
R23 R113
R29 R126
R38 R235
R92 R244
R99
680Ω
R71
R73
R115
1.5K

4. ALL CAPACITORS ARE µF.
3. ALL DIODES ARE FD6666.
2. ALL RESISTORS ARE IN OHMS.
1. PATIAL REFERENCE DES SHOWN. PREFIX WITH ASSEMBLY REF DES A6.

NOTE: UNLESS OTHERWISE SPECIFIED

7. * = NOMINAL VALUE CALLED OUT ON PARTS LIST

PART NUMBER WAS 1104-00-3277

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. LISSA SMITH	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR J. Z. Nauen	7/16/90	TITLE (A6) SCHEMATIC FREQUENCY BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV K. Wicks		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1104-00-3397 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 7

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3004

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REV	ECN	BY	DATE	APP

C210 5pf

U121 1/4 10H350

÷25 (REF)

20MHZ (4B3) TO µP

+5V

CR5

R30 750

R25 499

R26 1.21K

R27 249

C19 .01

GO BURST (1C1)

C18 .1

U28 10116

U29 10131

U31 10102

R22

U30 10131

R23

U25 10131

U24 10131

R29

4 MHZ CLK (3A7)

U18-10 (1C8)

÷25 (VARIABLE FREQ)

U115-14(7C7) 100MHz

U115-15 (7C7)

U32 10231

U33 10231

U26 10131

R111(5B6) 100-150MHz

C21 .01

C20 .1

C194 15pf

4-6MHZ OUT U3-3 (1B8)

J54

1 MRST
2
3 -15V
4 NC
5 NC
6 +5V
7
8 +15V
9 FUNCOUT (3C2)
10 FNCTST (3C7)

(3B6) BE

(3C4) RW/

C201 .1/50V

U120 74LS00

WE/

SQUAREWAVE AMP

CR8

C22 .01

R36 499

R37 499

R38

U37-2 (7C1)

U36 10102

R40 51.1

J10A

J10

R46 1.21K

R47 1.21K

U6-8 (1C1)

U2-11, U5-2 (1B8)

SWEEP RAMP GENERATOR

R34 1.5K

RST SW (1D5)

R35 2.49K

Q3 2N3640

Q4 2N5485

R39 200

C23 1uf ±1%

R41 15K

C24 .01

R44 100

U17 LF356

C25 .01

C26 .01

R45 619

SWEEP OUT

0-50MHz TO E14 & E15 OUTPUT POWER SUPPLY BD. (A4)

C177 .1/50V

R42 2.49K

R43 619

(3C2) RAMP STEP

Q5 2N3640

Q6 2N5771

R48 5.23K

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE 7/21/87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: FREQUENCY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX .030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 178 · DWG NO 1104-00-3397 · REV A
	SCALE		CODE IDENT 23338 · SHEET 2 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

µP 2 CONTROL CIRCUIT

(A7) µpCLOCK

(74LS373) U55

U44 27128

U45 61161 8000-61-1600

D7 D6 D5 D4 D3 D2 D1 D0

U42 6803

P17 HOLD/ (B4)
P16 ENABLE SWEEP STEP (B2)
P15 ENABLE INT (B3)
P14 SWEEP ENABLE (B2)
P13 EVENT SELECT 2 (A3)
P12 EVENT SELECT 1 (A3)
P11 ACCUMULATOR COMMAND 2 (A3)
P10 ACCUMULATOR COMMAND 1 (A3)

U52 825153 (FPLA)

U53 74LS74

U41 74LS 373

J13 BD7 … BD0 TO 1A8

U43 6840

U64 74LS00

U48 74LS86

U49 74LS175

U50 74LS08

U46 74LS138

J13
9 ATTN
10 OFST HI
11 OFST LO
12 AMPL
13 WAVE
14 NC.

(2B8) FUNCOUT
(C8) LOCK SENSE
+5V
ISO GND
+44V ISO

EP RESET/ (B3)

RAMP STEP (2A3)

U74-4 (A5)

U75 74LS109

SMCLOCK (4C7)

(4D7) SWEEP STEP/

ENABLE SWEEPSTEP (C6)

STORED SETTINGS/ TEST CONNECTOR J38

U51 74LS 163

U73 74LS390

U57 74LS157

U58 74LS244

U56 74LS75

U59 7404

U63 74LS151

U62 74LS74

U76 LS00

U47 74174

R71

R70 1K

GO SWEEP (B5) (IC7)

EVENTINT/ (D7)

LOAD FREQUENCY/ (4C6)
ENTER FREQUENCY/ (4C7)
LOAD INCREMENT (4C7)

(4C7) SM CLOCK

J15

ISO GND
+5V ISO
ISO GND
N.C.
+44V ISO

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE 2/17/88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJECTS		TITLE: SCHEMATIC FREQUENCY BD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO. 1104-00-3397 REV A
	SCALE	CODE IDENT 23338	SHEET 3 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3994

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REV	ECN	BY	DATE	APP

FREQUENCY CONTROL LOGIC

WRITEDATA 3/
WRITEDATA 2/
WRITEDATA 1/
WRITEDATA Ø/
(3B5,B6)
LOAD INCREMENT (3A2)
+5V
C38 .1/50V
U68 74LS157
3D6
U70 74S189
WRITELOAD/ (3C4)
C1
(3B1) SWEEP STEP/
(3A2) ENTER FREQUENCY/
U77 LS00
UPDATE FREQUENCY (D4)
U78 LS00
LOAD INCREMENT (3A2)
FRQCLK (D4,D5)
U85 74S189
(D7)
MCLK/(B1)
MCLK1 (B1)
(A7) CS3
(B7) CS2
(B5) CS1
C3 (A8,A6)
C2 (B7)
C1 (B5)
U65 74LS163
STOP (D2)
SM CLOCK (3C2,3A2)
MSDTIME (C2)
+5V
C163 .1/50V
U86 74LS75
(B1) MCLK1
(3A2) LOAD FREQUENCY/
U84 LS08
(C7) C2
U87 74LS283
CS2 (C7)
R75 1K
U77 LS00
LDBN (C2)
NEW FREQ 3 (D5) 18
NEW FREQ 2 (D5) 17
NEW FREQ 1 (D5) 14
NEW FREQ Ø (D5) 13
U89 74LS273
DBN7
DBN6
DBN5
DBN4
DBN3
DBN2
DBN1
DBNØ
(6C7)
(5B6)
(5A6)
(6C7)
C45 .1/50V
WRITEDATA 3/
WRITEDATA 2/
WRITEDATA 1/
WRITEDATA Ø/
(D7)
WRITEMARKER/ (3C4)
U69 74S189
MAR 3
MAR 2
MAR 1
MAR Ø
(D4)
C48 .01
MARKER GENERATOR
(C7) C3
U83 74LS283
CS3 (C7)
C49 .1/50V
(C2) LMARK
U88 LS74
CR11
CR12
R81 5.1
E35
J53
TO "MARKER OUT" REAR PANEL U25
(B7) NEW FREQ Ø
NEW FREQ 1
NEW FREQ 2
NEW FREQ 3
U81 74S189
FRQCLK (C6)
(C1)
C39 .1/50V
FREQCLK (C6)
U72 74S189
MAR3 (B6)
MAR2 (B6)
MAR1 (B6)
MARØ (B6)
C40 .1/50V
UPDATE FREQUENCY (D6)
U71 74LS157
D7
C1
SAMP Ø
SAMP 1
SAMP 2
SAMP 3
(3A7)
C41 .1/50V
U90 74LS75
MCLK2 (B1)
NEWPH3
NEWPH2
NEWPH1
NEWPHØ
(B5)
U80 74S189
MCLK1 (B1)
(C1)
U79 74LS75
MCLK2 (B1)
C1 (C7)
U82 74LS283
CS1 (C7)
NEWPH3
(D3)
U91
(B5,6C6)
(B4)
DAC 14
DAC 13
DAC 12
DAC 11
DAC 10
DAC 9
DAC 8
DAC 7
74LS273
U92
DAC 6
DAC 5
DAC 4
DAC 3
DAC 2
DAC 1
DAC Ø
OVERFLOW (5A6)
(6C6)
ADD CYCLE/ (5B1)
U78 LS00
U64 LS00
STOP (C7)
UPDATE FREQUENCY (D4,D6)
U66
U67 74LS163
MSD TIME (C6)
L MARK (A6)
L DAC (C4)
L DBN (B6)
MCLK1 (B1)
R72 1K
R73 1.5K
C43 .1/50V
C44 22/16V
AABØ
AAB1
AAB2
AAB3
(D7, D5, D3, C7')
MCLK/ (B1)
LDAC (C2)
6.67 MHz CLOCK
R76 1K
(2D3) 20MHZ
U60 74LS109
U59 7404
MCLK1
MCLK2
MCLK/

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN MELISSA SMITH
DATE 7/1/84
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC: FREQUENCY BOARD (A6)

MODEL NO 178
DWG NO 1104-00-3397
REV A
CODE IDENT 23338
SHEET 4 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

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SYNTHESIZER PHASE LOCK LOOP

REV	ECN	BY	DATE	APP

+5V-1
R85 200
J52
500KHz TO J2 REF. BD.
C51 .01
U110 10116
R90 499
R91 499
R92
C57 .01
U108 10116
PDELOUT 1
PDELOUT 2
(6A)
R99
U109 MC 12040
R92
+15V-3
C182 2.2/15V
C53 .1/50V
R93 499
C54 .01
R96 4.99K
R95 1.5K
CR15
CR16
CR17
CR18
HP2811(4)
R100 750
R97 76.8K,1%
C58 .0022
R101 11.8K
U111 LF356
-15V-3
R102 3.01K
R103 3.01K
R104 3.01K
R106 8.25K
R107 4.32K
C63 .1/50V
C64 .01
R109 499
CR19
R108 49.9K
+15V-2
C59 390pf SM
C60 390pf SM
C62 220 pf SM
R82 24.9K
R83 15K
R84 10K
C50 100/16V
C61 .1/50V
CR13
CR14
R88 100K
R89 4.99K
C55 .1/50V
R94 4.99K
U103 LF356
C52 .01
R86 30.1K
R87 1K
C56 .001
PRE-TUNE J1-1 VCO BD.
R98 1K
U114 LF356
R105 1K
FINE TUNE J1-3 VCO BD.
U93 10116
+5V
R110 200
C65 .1/50V
CR20
R111 33.2
100-150MHz U32-6 (2C7)
Q8 2N3640
R126
C66 .01
1.5K
R112 54.9
+5V-1
C67 .1/50V
R115
1.62K(4)
DBN7
DBN6
DBN5
DBN4
R116
R117
R118
R119
(4B7)
U94 10231
÷100-150
U95 10136
PROGRAMMABLE ÷N COUNTER
100-150 MHz TI OUTPUT (7B8)
R124 200
R125 200
R126 680Ω
C70 .1/50V
R114
1.5K
DBN3
DBN2
DBN1
DBN0
R127
R128
R129
R130
U96 10136
10105
U97
R132 301
R133 499
TP1
CR21
OVERFLOW (4A4)
U94 10231
R113 680Ω
U98 10136
U99 10116
PDELIN 2
PDELIN 1
(6AB)
R120 150
C69 .1/50V
C68 .1
R122 100
R121 33.2
R123 33.2
Q9 2N3640 (2)
Q10
ADD CYCLE (4D2)
R131 301

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN MELISSA SMITH
DATE 7/21/89
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC: FREQUENCY BOARD (A6)

MODEL NO 178
DWG NO 1104-00-3397
REV A
CODE IDENT 23338
SHEET 5 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3894

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REV	ECN	BY	DATE	APP

PHASE DELAY CURRENT GENERATOR

HI FREQ SPUR COMPENSATION

LEVEL DETECTOR

PHASE DELAY RAMP GENERATOR

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE 7/21/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: FREQUENCY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE/ APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178
	SCALE		DWG NO 104-00-3397 REV A
			CODE IDENT 23338 SHEET 6 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3954

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REV	ECN	BY	DATE	APP

AMPLITUDE TEMP COMP

REF BUFFER AMP

MIXER/BUFFER AMP

SQUARE AMP

100MHz FILTER

60MHz FILTER

LO FREQ AMP

POWER SUPPLY DISTRIBUTION

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN MELISSA SMITH	DATE 7/13/89	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: FREQUENCY BOARD (A6)
	RELEASE/ APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1°		
	DO NOT SCALE DWG		MODEL NO 178 · DWG NO 1104-00-3397 · REV A
	SCALE		CODE IDENT 23338 · SHEET 7 OF 7

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3094

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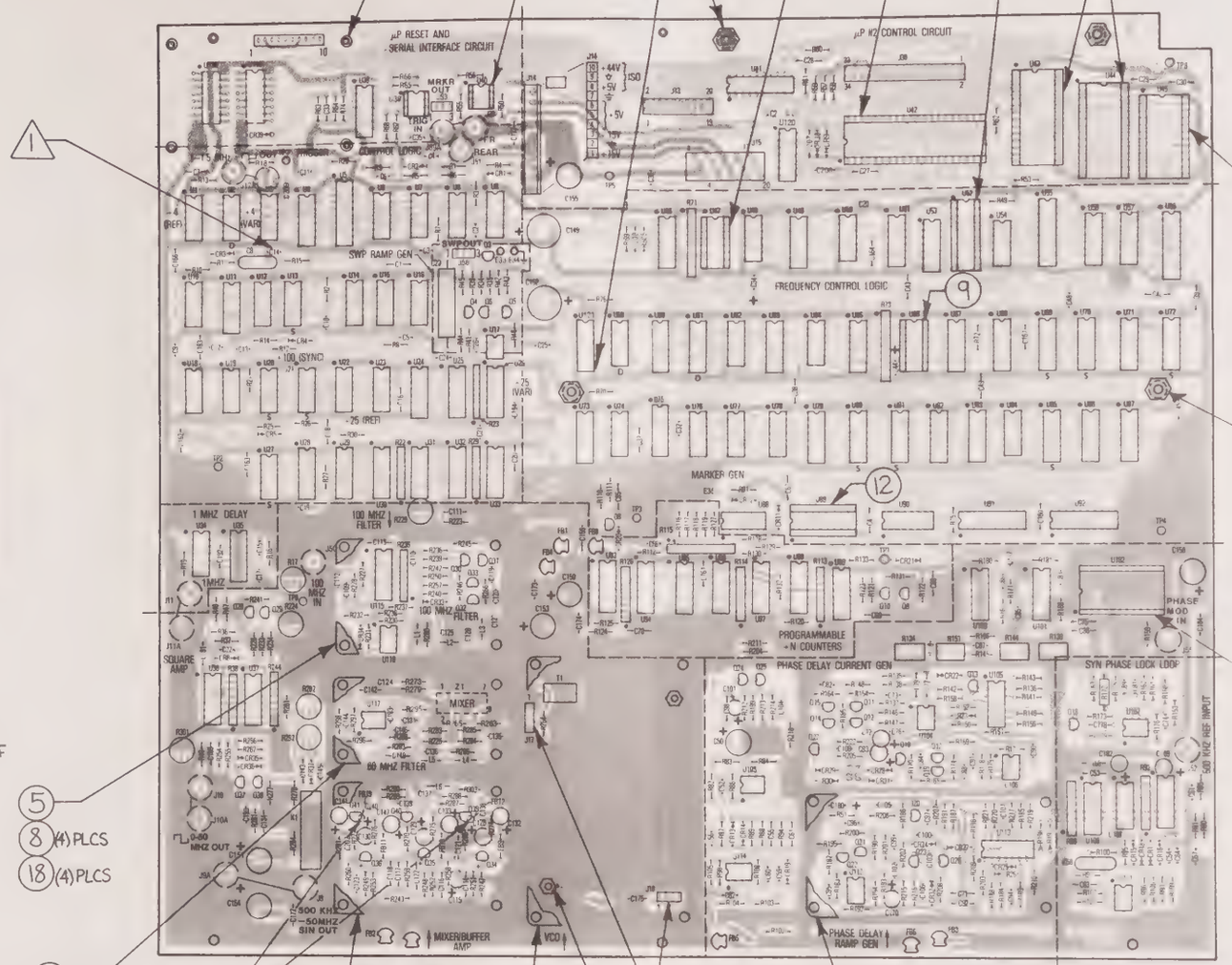
REV	ECO	BY	DATE	APP
A	ECO#90-343	MS	3/28/90	K.J.

C210 IS INSTALLED IN THIS LOCATION ON THE CIRCUIT SIDE SEE DETAIL "A".

(4)PLCS (8)
(4)PLCS (18)

(14) (16)(2)PLCS (9) (11) (12) (13)



(1)

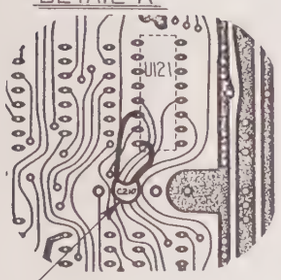
(10)

(16)(2)PLCS

(12)

(9)

DETAIL "A"



ONE LEAD OF C210 TO BE SOLDERED TO PIN #9 OF U121, THE OTHER LEAD OF C210 TO BE SOLDERED TO PIN # 11 OF U121 ON THE CIRCUIT SIDE OF THE BOARD.

(5)
(8) (4)PLCS
(18) (4)PLCS

(6)
(8) (4)PLCS
(18) (4)PLCS

(2)

(7)
(8) (4)PLCS
(18) (4)PLCS

(3)
(16) (4)PLCS
(18) (4)PLCS

(15) USE 4 EACH (2)PLCS TYP.

(17) (2)PLCS
(2)
(18) (2)PLCS

(4)
(8) (4) PLCS
(18) (4)PLCS

3. INSTALL SPRING SOCKET REF. DES. 20 AT J9A, J10A, J11A, J12A, J39A.

2. INSTALL FERRITE BEAD P/N 3100-00-0001 ON THE BASE LEAD OF Q39 AND Q41

1. NOMINAL VALUE CALLED OUT ON P/L.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Melissa Smith 3-28-90	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	CHECKED D. Buzzelli 4/5/90	TITLE ASSEMBLY FREQUENCY GENERATOR BD.	
FINISH WAVETEK PROCESS	PROJ. ENGR Frank Fo 4/5/90		
DO NOT SCALE DRAWING	RELEASE APPROV Frank Fo 4/5/90	SIZE D	FSCM NO 23338
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES . XX ; XXX .	DWG NO 1101-00-3397	REV B
		SCALE FULL	MODEL 178
		SHEET 1 OF 1	

REV	ECN	BY	DATE	APP

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT & CABLE ROUTING	0004-00-0279	WVTK	0004-00-0279	1
NONE	A/D FREQUENCY GENERATOR BD	1101-00-3397	WVTK	1101-00-3397	1
NONE	SCHEMATIC FREQUENCY GENERATOR BD	1104-00-3397	WVTK	1104-00-3397	1
NONE	CABLE KIT FOR 178 STD FREQ/GEN BOARD	1200-00-3398	WVTK	1200-00-3398	1
T1	TRANSFORMER	172-537	WVTK	1204-00-0537	1
2	ASSY VCO BD	1208-00-2642	WVTK	1208-00-2642	1
5	SHIELD, 100 MHz FILTER (OPT-010)	1400-02-0793	WVTK	1400-02-0793	1
6	SHIELD, 60MHz FILTER (OPT-010)	1400-02-0803	WVTK	1400-02-0803	1
7	SHIELD, MIXER BUFFER AMP (OPT-010)	1400-02-0813	WVTK	1400-02-0813	1
3	SHIELD, VCO BD (OPT-010)	1400-02-0823	WVTK	1400-02-0823	1
4	SHIELD, PHASE DELAY (OPT-010)	1400-02-0833	WVTK	1400-02-0833	1
C119 C210 C35	CAP, CER DISK, 5PF, 1KV, 10%	0311-00018	WVTK	1500-00-5011	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C6	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C104 C190 C2 C209 C4 C5 C81 C90	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	8
C12 C146 C193 C3 C56 C74 C95 C96	CAP, CER, .001UF, 1KV	DD-102	CRL	1500-01-0211	8
C103 C106 C107 C108 C109 C11 C110 C112 C120 C131 C145 C157 C17 C19 C21 C22 C24 C25 C26 C32 C48 C51 C52 C54 C57 C64 C66 C73 C76 C78 C82 C83 C84 C85 C86 C87 C89 C9 C91 C94 C97	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	41
C1 C111 C113 C114 C116 C117 C118 C134 C142 C143 C148 C156 C16 C160 C161 C162 C163 C164 C165 C166 C167 C168 C172 C173 C174 C175 C177 C178 C179 C18 C183 C184 C191 C192 C20 C201 C27 C28 C29 C30 C31 C33 C37 C38 C39 C40 C41 C43 C45 C49 C53 C55 C61 C63 C65 C67 C68 C69 C7 C70 C71 C75 C77 C79 C80 C92 C98	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	67
C194	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	1
C10 C36 C88	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C200	CAP, CER DISK, 33PF, 1KV, 10%	50A033	SPRAG	1500-03-3001	1
C206 C207	CAP, CER, 33PF, 100V+-5%, AXIAL	CAC02CD0330J100A	CORNG	1500-03-3006	2
C102 C144 C99	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	3
C13	CAP, CER, 68PF, 1KV	DD-680	CRL	1500-06-8001	1
C105 C136 C137	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	3
C203 C204	CAP, MICA, 15PF, 500V	DM15-150J	ARCO	1500-11-5000	2
C100 C208	CAP, MICA, 150PF, 500V	DM15-151J	ARCO	1500-11-5100	2
C14T	CAP, MICA, 180PF, 500V	DM15-181J	ARCO	1500-11-8100	1
C62	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
C202	CAP, MICA, 270PF, 500V	DM15-271J	ARCO	1500-12-7100	1
C139	CAP, MICA, 300PF, 500V, RADIAL	DM15-301J	ARCO	1500-13-0100	1
C124 C127	CAP, MICA, 36PF, 500V	DM15-360J	ARCO	1500-13-6000	2
C135 C138	CAP, MICA, 39PF, 500V	DM15-390J	ARCO	1500-13-9000	2
C59 C60	CAP, MICA, 390PF, 500V	CD15-391J	CDE	1500-13-9100	2

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C125 C126 C15	CAP, MICA, 56PF, 300V	DM15-560J	ARCO	1500-15-6000	3
C150 C153 C50	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	3
C149 C151 C152 C154 C155 C158	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	6
C23	CAP, POLYC, 1MF, 100V, AXIAL	B1A105F	ELPAC	1500-41-0504	1
C58 C8	CAP, MYLR, .0022MF100V	225P22291WD3	SPRAG	1500-42-2214	2
C121 C122 C123	CAP, TANT, 1MF, 35V	150D105X9035A2	SPRAG	1500-71-0502	3
C101 C115 C128 C129 C130 C132 C133 C141 C147 C169 C170 C180 C182 C34 C44 C72 C93	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	17
NONE	PCB, FREQUENCY GENERATOR BD 178-STD UPGRADE	1700-00-3397	WVTK	1700-00-3397	1
L4 L6	CHOKE, .18MH, 10%	1025-02	DLVAN	1800-00-0012	2
L2	INDUCTOR, .12MICRO H	1025-96	DELVN	1800-00-0019	1
L1 L3	INDUCTOR, .1 MICRO H	1025-94	DELVN	1800-00-0020	2
L5	INDUCTOR, .22 MICRO H	1025-04	DELVN	1800-00-0021	1
J14	CONN, HEADER	1-640386-0	AMP	2100-02-0079	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J33 J36	CONN, HEADER, 3 PIN, .100 MTA	640456-3	AMP	2100-02-0116	2
J34	CONN, HEADER, SINGLE ROW, 10 PIN 0.1 SPACE	535541-8	AMP	2100-02-0215	1
9	SKT, IC, 16PIN	DILB16P-108T	BURND	2100-03-0028	2
10	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	2
11	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	1
'J12A J10A J11A J39A J9A	CONN, COAX SOCKET	226287-2	AMP	2100-03-0038	5
20	SPRING SOCKET	50935-1	AMP	2100-03-0039	5
12	SOCKET, 20 PIN	DILB20P-108T	BURND	2100-03-0051	3
13	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	2
14	SOCKET, 8 PIN	DILB08P-108T	BURND	2100-03-0063	1
E33 E34 E35	PIN, MALE	60809-2	AMP	2100-05-0020	3
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	8
15	CONN PIN, MALE (UOM-EA PIN)	CA-S36SP-100-230-830	CA	2100-05-0034	8
J38	CONN, HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J13	CONN, HEADER, 20 PIN	929836-01-10	AP	2100-05-0042	1
J10 J11 J12 J39 J50 J51 J52 J55 J9	CONN, SMB, MALE JACK RECEPTACLE PERPENDICULAR PC MOUNT, SNAP FIT	221111-1	AMP	2100-11-0002	9
16	STANDOFF, SWAGE .625 H, X 250DIA 6-32, 062 MATL	1531B-5/8	USECO	2800-02-0004	8
17	STANDOFF, SWAGE .250 H, .250 HEX 6-32, .062 MATL	B1531B-1/4-11	USECO	2800-02-0022	2
8	STANDOFF SWAGE, 1/4 RND, .0.062 MATERIAL, THREAD THRU 6-32X7/16 LONG	AL6910B-437-00	LNTRN	2800-06-0041	20
18	SCREW, 6-32X5/16 PHP, NYLOK PATCH, Z PATCH, 6-32 X 5/16	6-32X 5/16 NYLOK	CMRCL	2800-23-6105	26
FB10 FB11 FB12 FB13 FB9	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	5
FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8	BALUN CORE	2873000902	FARIT	3100-00-0002	8
K1	RELAY, REED, FORM-C	RA30571051	ETROL	4500-00-0009	1
R17 R224 R282	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, FREQUENCY GENERATOR BD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 178 / DWG NO 1100-00-3397 / REV A
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 3
	SCALE		

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27089

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R292	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	1
R301	POT, TRIM, 500	91AR500	BECK	4600-05-0104	1
R144	POT, TOP TRIM, 20T, 10K	68WR10K	BECK	4609-90-0002	1
R139	POT, TOP TRIM, 20T, 2K	68WR2K	BECK	4609-90-0004	1
R151	POT, TOP TRIM, 20T, 5K	68WR5K	BECK	4609-90-0013	1
R134	POT, TOP TRIM, 20T, 100	68WR100	BECK	4609-90-0019	1
R229	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	1
R122 R14 R146 R166 R167 R18 R184 R185 R19 R201 R203 R207 R208 R212 R217 R222 R242 R246 R270 R44 R69	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	21
R105 R155 R161 R221 R256 R262 R277 R49 R61 R64 R70 R72 R74 R75 R76 R87 R98	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	17
R1 R138 R145 R152 R178 R183 R200 R202 R225 R297 R299 R57 R58 R62 R84	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	15
R55 R63 R65 R66 R67 R68 R86	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	7
R204 R211 R223 R243 R288 R290 R291	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	7

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R232	RES, MF, 1/8W, 1%, 10.5K	RN55D-1052F	TRW	4701-03-1052	1
R101	RES, MF, 1/8W, 1%, 11.8K	RN55D-1182F	TRW	4701-03-1182	1
R273	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701-03-1210	1
R26 R46 R47 R5	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	4
R159	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	1
R272	RES, MF, 1/8W, 1%, 124	RN55D-1240F	TRW	4701-03-1240	1
R120 R193 R195 R213 R264 R265 R285 R286	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	8
R179 R34 R95	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	3
R147 R164 R169 R170 R251 R252 R253 R41 R83	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	9
R233 R234	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	2
R116 R117 R118 R119 R127 R128 R129 R130	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	8
R50	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R142 R150 R158	RES, MF, 1/8W, 1%, 19.1K	RN55D-1912F	TRW	4701-03-1912	3
R110 R124 R125 R177 R241 R259 R278 R303 R305 R39 R85	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	11
R182 R218 R39	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R237 R240	RES, MF, 1/8W, 1%, 21.5K	RN55D-2152F	TRW	4701-03-2152	2
R250 R257	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R148 R173 R174 R209 R210 R239 R254 R255 R27 R276 R3 R6 R7 R8 R9	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	15
R13 R141 R190 R191 R2 R20 R21 R219 R220 R236 R245 R281 R35 R42 R56 R60	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	16
R82	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R206	RES, MF, 1/8W, 1%, 24.9	RN55D-24R9F	TRW	4701-03-2499	1
R16T	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	1
R131 R132 R214 R268	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	4
R102 R103 R104 R137 R188 R189 R194 R205 R231 R261 R283	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	11
R192 R86	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	2
R293	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R11 R12	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	2
R4	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 9

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R111 R121 R123 R197 R198	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	5
R238	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R263 R284	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	2
R287	RES, MF, 1/8W, 1%, 42.2	RN55D-42R2F	TRW	4701-03-4229	1
R107	RES, MF, 1/8W, 1%, 4.32K	RN55D-4321F	TRW	4701-03-4321	1
R258 R274	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	2
R230	RES, MF, 1/8W, 1%, 46.4K	RN55D-4642F	TRW	4701-03-4642	1
R10 R109 R133 R15 R162 R176 R25 R296 R298 R36 R37 R53 R90 R91 R93	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	15
R136 R143 R149 R154 R156 R157 R165 R196 R247 R248 R249 R302 R51 R89 R94 R96	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	16
R108 R295	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	2
R227 R228 R266 R294 R40 R81	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	6
R48	RES, MF, 1/8W, 1%, 5.23K	RN55D-5231F	MEPCO	4701-03-5231	1
R112	RES, MF, 1/8W, 1%, 54.9	RN55D-54R9F	TRW	4701-03-5499	1
R260	RES, MF, 1/8W, 1%, 59	RN55D-59R0F	TRW	4701-03-5909	1
R43 R45	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	2

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R175 R199	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	2
R100 R135 R187 R216 R30	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	5
R168 R171 R180 R181 R186 R215	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	6
R97	RES, MF, 1/8W, 1%, 76.8K	RN55D-7682F	TRW	4701-03-7682	1
R275	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R106	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R153 R160	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	2
R163T	RES, MF, 1/8W, 1%, 9.53K	RN55D-9531F	TRW	4701-03-9531	1
R172	RES, MF, 1/4W, 1%, 1M	RN60D-1004F	TRW	4701-13-1004	1
R226 R279 R280	RES, MF, 1/4W, 1%, 71.5	RN60D-71R5F	TRW	4701-13-7159	3
R115 R71 R73	RES NETWORK 1.5K 2% 10PIN SIP BUSS	785-1R1.5K	BECK	4770-00-0010	3
R113 R114 R126 R22 R23 R235 R244 R29 R38 R92 R99	RES NETWORK 68002% 8PIN SIP BUSS	4308R-101-681	BOURN	4770-00-0031	11
CR32	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A	1N751A	FAIR	4801-01-0751	1
CR25 CR26 CR35 CR36	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	4

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 11

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR1 CR11 CR12 CR13 CR14 CR19 CR2 CR20 CR21 CR22 CR23 CR3 CR33 CR34 CR37 CR38 CR4 CR5 CR8 CR9	DIODE 1N4148 COMPUTER, Q/P, 75V, 200M A, SWITCHING	1N4148	FAIR	4807-02-6666	20
CR15 CR16 CR17 CR18 CR24 CR27 CR28 CR29 CR30 CR31 CR39	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	11
Q23 Q37 Q38	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	3
Q10 Q3 Q5 Q8 Q9	TRANS, PNP, TO-92	MPS3640-005	MOT	4901-03-6400	5
Q17 Q19 Q21 Q22	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3903	NSC	4901-03-9030	4
Q11 Q12 Q30 Q31 Q34 Q35 Q36	TRANS, GENERAL PURPOSE, PNP, TO-92	2N3905	ITT	4901-03-9050	7
Q14 Q18	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	2
Q13 Q16 Q4	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	3
Q6	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	1
Q15 Q20 Q24 Q25 Q26 Q27 Q28 Q29 Q32 Q33	TRANS, PNP, TO-92	MPS-L08	FAIR	4902-00-0080	10
Q39 Q40 Q41	TRANS	NE41632E-1-D	CEL	4902-02-1320	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A | PAGE 12

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, FREQUENCY GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-3397 REV A
	SCALE	CODE IDENT 23338	SHEET 2 OF 3

BISHOP GRAPHICS ACCURPRESS REORDER NO. A27088

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
J15	ASSY, RIBBON CABLE 20 PIN X 22 LONG	6002-00-0013	WVTK	6002-00-0013	1
U100 U101	DAC, 8BIT HI-SPEED MULT	DAC-08EQ	AMD	7000-00-0800	2
U105	OP AMP, QUAD MC1741 DIFFERENTIAL INPUT	LM348N	NSC	7000-03-4800	1
U103 U104 U106 U107 U111 U112 U114 U117 U17	OP-AMP	LF356N	NSC	7000-03-5600	9
U39	COMPARATOR, LOW POWER LOW OFFSET VOLTAGE DUAL	LM393N	NSC	7000-03-9300	1
U102	DAC, MONOLITHIC, HIGH SPEED, 12 BIT	AD565AJD/BIN	AD	7000-05-6500	1
U116	OP AMP, INTERNALLY COMP, HIGH PERFORMANCE	LM741CN	NSC	7000-07-4100	1
U113	TRANS ARRAY, HIGH FREQ, NPN	CA3127E	RCA	7000-31-2700	1
U43	PROGRAMMABLE TIMER	MC6840P	MOT	7000-68-4000	1
U95 U96 U98	COUNTER, UNIV HEX, ECL	HD10136P	HTACH	7001-01-3600	3
U40	OPTO CPLR, FAST	6N136	SPECT	7100-00-0001	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	INP, TTL				
U20 U21	FLIP-FLOP DUAL D- POS EDGE TRIG	74874	TI	8000-74-7401	2
U1 U14 U3 U34 U53 U62 U74 U88	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	8
U56 U79 U86 U90	LATCH, 4B BISTAB, TTL	74LS75	TI	8000-74-7510	4
U18 U48 U7	GATE XOR, QUAD 2INP, TTL	74LS86	TI	8000-74-8610	3
U31 U36	GATE, NOR, QUAD 2 INP, ECL	MC10102	MOT	8001-01-0200	2
U97	GATE, OR/NOR, 2-3--2INP, ECL	MC10105	MOT	8001-01-0500	1
U108 U110 U115 U28 U37 U93 U99	RCVR, TRI LINE, ECL	MC10116P	MOT	8001-01-1600	7
U24 U25 U26 U29 U30	FLIP-FLOP DUAL, ECL	MC10131	MOT	8001-01-3100	5
U32 U33 U94	FLIP-FLOP DUAL, D-HI SPEED, ECL	MC10231	MOT	8001-02-3100	3
U121	TRANSLATOR, ECL TO TTL	MC10H350P	MOT	8001-03-5000	1
U109	PHASE-FREQ DET, ECL	MC12040	MOT	8001-20-4000	1
U38	COUNTER, 12 BIT NIN,	14040	RCA	8001-40-4000	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U23	COUNTER, BCD, TTL	74LS290	TI	8007-42-9010	1
U41 U55	LATCH, OCTAL TRANSPAR W/3 STATE	74LS373	MOT	8007-43-7310	2
U73	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1
U66	IC, PROGRAMMED V1.0, REF: 8007-41-8801	8600-00-0201	WVTK	8600-00-0201	1
U47	IC, PROGRAMMED V1.0, REF: 8007-41-8801	8600-00-0202	WVTK	8600-00-0202	1
U52	IC, PROGRAMMED REF 8008-21-5300	8600-00-0340	WVTK	8600-00-0340	1
U44	IC, PROGRAMMED V2.5 REF 8002-71-2800	8600-00-0374	WVTK	8600-00-0374	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
Z1	IC, SEL, MD108 QTY: 1: 7000-01-0800	7200-00-0016	WVTK	7200-00-0016	1
U45	SRAM, 2KX8, 120NS, CMOPS	CXK5816PN-12L	SONY	8000-61-1600	1
U42	MICROPROCESSOR, 8BIT	MC6803L	MOT	8000-68-0300	1
U120 U19 U64 U76 U77 U78	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	6
U2	GATE, NAND, QUAD 2-INPUT POS W/DC OUTPUTS	SN7401N	TI	8000-74-0100	1
U27	GATE, NOR, QUAD 2-INPUT	74802	SIG	8000-74-0201	1
U10 U12 U15	GATE, NOR, QUAD, 2INP, TTL	74LS02	TI	8000-74-0210	3
U59	INVERTER, HEX	7404	TI	8000-74-0400	1
U54	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	1
U50 U84	GATE AND, QUAD 2-INP, TTL	74LS08	TI	8000-74-0810	2
U13	GATE, NAND, TRI 3-INPUT	74S10	SIG	8000-74-1001	1
U16 U8	GATE, NAND, 3 INP, TTL	SN74LS10N	TI	8000-74-1010	2
U22	GATE, NAND, DUAL, 4	74LS20	TI	8000-74-2010	1

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	CMOS				
U11 U60 U75	FLIP-FLOP, DUAL J-K, TTL	74LS109	SIG	8007-41-0910	3
U35	MULTVB, DUAL RTRG, TTL	74LS123	SIG	8007-41-2310	1
U6 U9	GATE, NAND, QUAD S/TRIG, TTL	74LS132	TI	8007-41-3210	2
U46	DECODER, 1-8 LINE, TTL	74LS138	TI	8007-41-3810	1
U4 U63	MUX, DATA, 1 OF 8, TTL	74LS151	TI	8007-41-5110	2
U57 U68 U71	MUX, QUAD, 2-INP, TTL	74LS157	TI	8007-41-5710	3
U51 U65 U67	COUNTER, SYNC 4-BIT, TTL	74LS163	SIG	8007-41-6310	3
U61	FLIP-FLOP, HEX D	74174	TI	8007-41-7400	1
U49	FLIP-FLOP, QUAD D, TTL	74LS175	TI	8007-41-7510	1
U69 U70 U72 U80 U81 U85	RAM, 16X4, 25NS, TTL	DM74S189AN	NSC	8007-41-8900	6
U58	BUF, OCT 3ST OUT, TTL	SN74LS244N	TI	8007-42-4410	1
U5 U89 U91 U92	FLIP-FLOP, OCT D, TTL	74LS273	TI	8007-42-7310	4
U82 U83 U87	ADDER, FULL 4-BIT, TTL	74LS283	TI	8007-42-8310	3

WAVETEK PARTS LIST | TITLE: PCA, FREQUENCY GENERATOR BD 178-STD | ASSEMBLY NO. 1100-00-3397 | REV A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, FREQUENCY GENERATOR BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 1100-00-3397 / REV A
	SCALE		CODE IDENT 23338 / SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A2708

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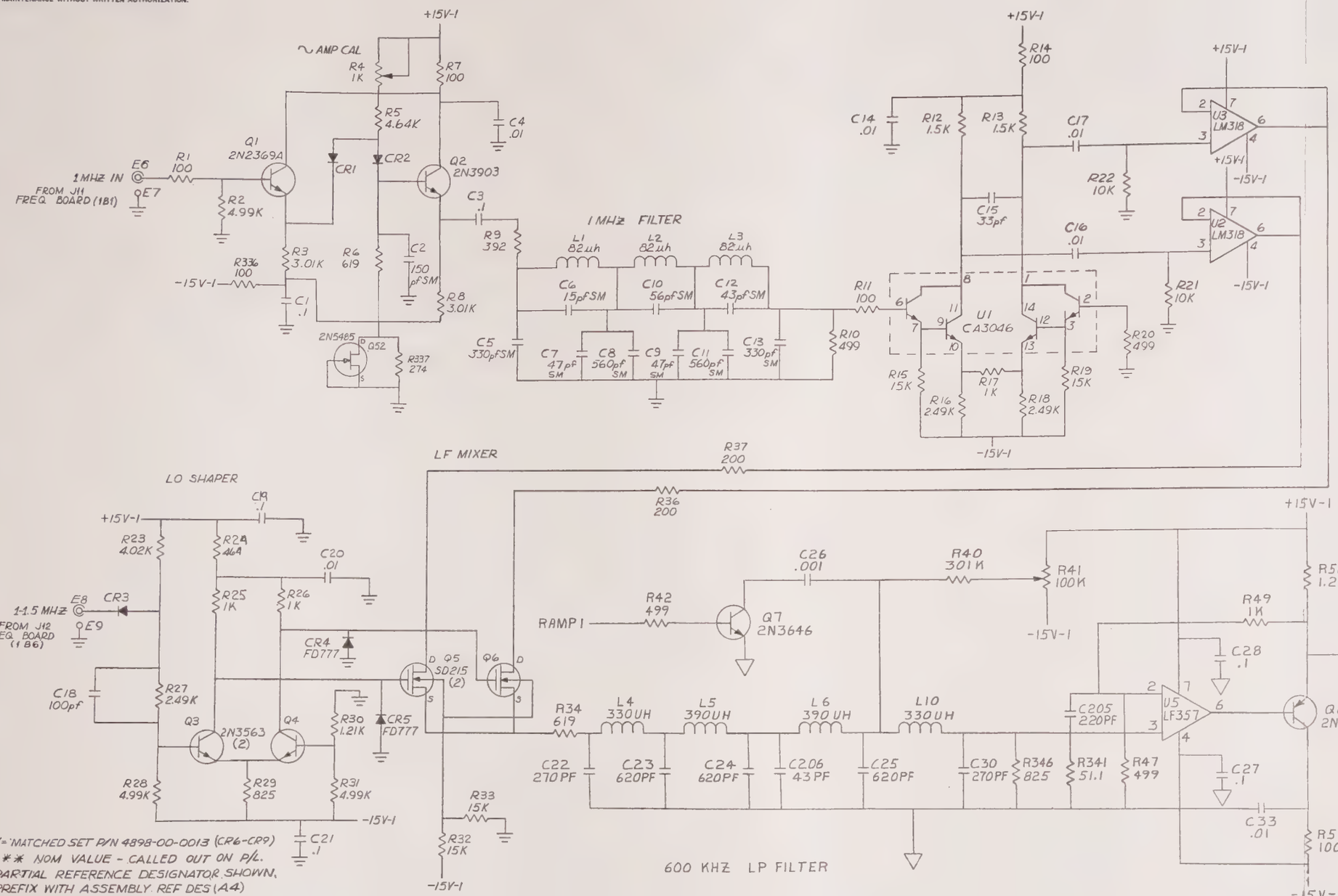
REV	ECN	BY	DATE	APP
F	ECN 2710	LOU	5/13/81	
G	ECN 2781 2690 2776, 2745	DC	8/26/81	
H	ECN 2830	FNA	9-14-81	
J KL	2° CONFIGURATION	BO	1-23-82	
M	2725, 3019	BO	1-23-82	
N	3103, 3119	FNA	3-16-82	
P	3125	FNA	3/31/82	
Q	ECN 3427	RO	8-9-82	
	ECN 3428 (CL III)	DC	12-10-82	
R	ECN 3353	DC	12-10-82	
S	ECN 3469, 3626	DC	12-10-82	
T	ECN 3587	DC	2-8-83	
U	ECN 3690	FNA	5/10/83	
V	# 3863	SC	7/14/83	
W	ECN #4128	RO	1/84	
Y	#4206, 4207 & 4209	RO	3/84	
Z	#4512, 4537, 4735 & 4706	[illegible]	[illegible]	
AA	7423	L. Sullivan	8/4/86	
AB	7653	BR	11/18/86	
AC	7814	BR	12/12/86	
AD	7785	BR	1/15/87	
AE	# 9035	[illegible]	8/1/91	
	B9-423	BG	9.89	



11. Ø = MATCHED SET P/N 4898-00-0013 (CR6-CR9)
10. ** NOM VALUE - CALLED OUT ON P/L.
9. PARTIAL REFERENCE DESIGNATOR SHOWN, PREFIX WITH ASSEMBLY REF DES (A4)
8. ALL CAPACITORS ARE IN uf
7. △ = 1/4 W, 1%
6. ∮ = MATCHED SET P/N 4789-00-0047 (R152 THRU R157)
5. ⊕ = MATCHED PAIR P/N 4789-00-0019 (R323-R324)
4. ⊕ = MATCHED PAIR P/N 4789-00-0019 (R310-R311)
3. * = MATCHED PAIR P/N 4789-00-0019 (R214-R278)
2. ALL DIODES ARE FD6666.
1. ALL RESISTORS ARE IN OHMS.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S CHERMACK 3-2-80
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC: OUTPUT/POWER SUPPLY BD. (A4)

MODEL NO 178 | DWG NO 0103-00-0752 | REV AE
CODE IDENT 23338 | SHEET 1 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3994

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REV	ECN	BY	DATE	APP

AM CIRCUIT

SYNC AND SQUARE WAVE SHAPER

PREAMP

TRIANGLE CONVERTOR

FUNCTION CONTROL LOGIC

BINARY ATTENUATOR

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: OUTPUT/POWER SUPPLY BD. (A4)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 178 · DWG NO 0103-00-0752 · REV AE
	SCALE		CODE IDENT 23338 · SHEET 2 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3854

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REV	ECN	BY	DATE	APP

POWER AMPLIFIER

+15V-2 · -15V-2 · 21.5(8)

R180 4.99K · R177 15K · R178 15K · R179 7.5K · U23 µA741 · C93 470pf · C94 470pf · R196 4.99K · R345 3.01K · R194 4.99K · R195 150 · Q24 2N2905A · R197 200

R221 · C203, 100pf · R223 · R222 · R224 · R225 · R226 · R227 · R228 · C230 100PF · C108 .1 · C109 100µf/16V

R203 5.76K · R204 5.76K · R205 27 1/2W · R206 27 1/2W · C95 .01 · C96 .01

R172 3.32K · R176 3.32K · R181 7.5K · R191 499 · C86 .1 · R182 100 · Q22 2N5771 · FB11 · Q25 µA400 · C85 .01 · C87 .01 · R192 274 · R184 10K · R183 90.9 · CR26 · C79 · U22 · CA3096 · C81 .001 · R185 392 · C82 .47µf · FB10 · Q26 µA400 · C88 .01 · Q23 2N5771 · C89 5pf · C90 .1 · R186 7.5K · R174 100 · R175 3.32K POWER AMP OFFSET · C208 .001 · R173 499 · STABILITY · R193 750 · R194 100

R207 21.5 · R208 750 · C97 ** · C98 35pf · R238 750 · R212 200 · C99 .022 · R216 21.5 FOLY.KS · R209 49.9 1/4W · R210 49.9 1/4W · R211 49.9 1/4W · R214 49.9 1/4W · R213 49.9 1/4W · R215 49.9 1/4W · Q28 2N3866 · Q29 2N5583 · R229 10 · R230 10 · Q30 2N5160 · Q32 2N5160 · C100 .1 · C101 .1 · C102 .1 · C103 .1 · Q31 2N3866 · Q33 2N3866 · R231 10 · R232 10

R241 61.9 · C110 **

R242 49.9 1/4W K4 · K5 · K6

R201 200 · C104 .01 · R217 27 1/2W · R218 27 1/2W · C105 .01 · R219 5.76K · R220 5.76K · R233 · R234 · R235 · R236 · R237 · R238 · R239 · R240 · C204 100pf · C106 .1 · C107 100µf/16V

R187 15K · R188 15K · R189 7.5K · U24 µA741 · C91 390pf · C92 470pf · R199 4.99K · Q27 2N2219A · R190 4.99K · R200 4.99K · R202 150 · PA SUM (2 C1)

OUTPUT ATTENUATOR

R247 124 · R248 124 · R254 124 · R253 124 · C245 15pf · R359 200 · R260 249 · R261 249 · R243 100 · R245 121 · R244 100 · R246 121 · R250 121 · R252 124 · R249 121 · R251 124 · R256 332 · R258 196 · R255 332 · R257 332 · R259 249K · R263 332 · R265 332 · R267 332 · R262 332 · R264 332 · R266 332 · R268 TBD

K7 · K8 · K9 · K10 · E18 · E19 · E29 · E30 · FUNC OUT REAR · FUNC OUT

+5V-1 · C112 1000µf/16V · C113 .1 · R282 10 · R283 10 · R284 10 · R285 10 · C123 .01 · C111 .01 · C119 .01 · C114 .01 · C120 .01 · C116 .01 · C121 .01 · C122 .01 · C124 .01 · R288 1K · Q34 2N3646 · R230 2K · R243 2K · R244 2K · E48 · E49 · E47 · U32 · U31 74LS374 · TO FREQ BD (3D1) · BD5 · BD4 · BD3 · BD2 · BD1 · BDØ · BD6 · BD7 · ATTEN (3 A7) · SYNC Ø (2 D5)

P7- J7-

1 BDØ · 2 BD1 · 3 BD2 · 4 BD3 · 5 BD4 · 6 BD5 · 7 BD6 · 8 BD7 — TO FREQ BD (3D1)

9 ATTN (3 B4) · 10 OFST HI · 11 OFST LO · 12 AMPL (2 B4) · 13 WAVE (2 B6) · 14 NC LOCK SENSE E28 · 15 NC · 16 NC · 17 · 18 · 19 NC · 20 NC — TO U13 FREQ BD

+5V-1 · +5V-2 · BD7 · BD6 · BD5 · BD4 · BD3 · BD2 · BD1 · BDØ · U25 74LS273 · U27 AD561J · MSB · U26 74LS175 · RAMP 1 (1A5)

DC GAIN ADJ · R273 200 · R274 10K * · R275 4.99K · R276 4.99K · R277 * · R278 0K * · R279 10K · C131 .01 · TP5 · TP4 · C128 10pf · C129 .1 · R270 15K · R269 301K · R271 100K · R272 4.99K · C127 .1 · DC OFFSET ZERO · U28 µA741 · U29 µA741 · U30 TL188CN

DC OFFSET CIRCUIT

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SCHERMA	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: OUTPUT/POWER SUPPLY BD.(A 4)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG SCALE	MODEL NO 178	DWG NO 0103-00-0752 AE
		CODE IDENT 23338	SHEET 3 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

+15V REG

+5V REG

REAR PANEL
E44
E45
E22 GND
+5V UNREGULATED
E23
3N254
P4- J4-
15VAC 10
(34 VRMS)
15VAC 9
GND 8
ISO +44V AC 7 6 5 4
(8.5 VRMS)
ISO +5VAC 3 2
(37.5VRMS)
N.C. 1 N.C.
TP6-9

-15V REG

+5 ISO REG

+ 44V ISO REG

POWER DISTRIBUTION

J8- P8-
10 +15V
5,6,7 +5V
9,7 GND
8 -15V
1 +44V ISO
3 +5V ISO
2 ISO GND

NOTE UNLESS OTHERWISE SPECIFIED

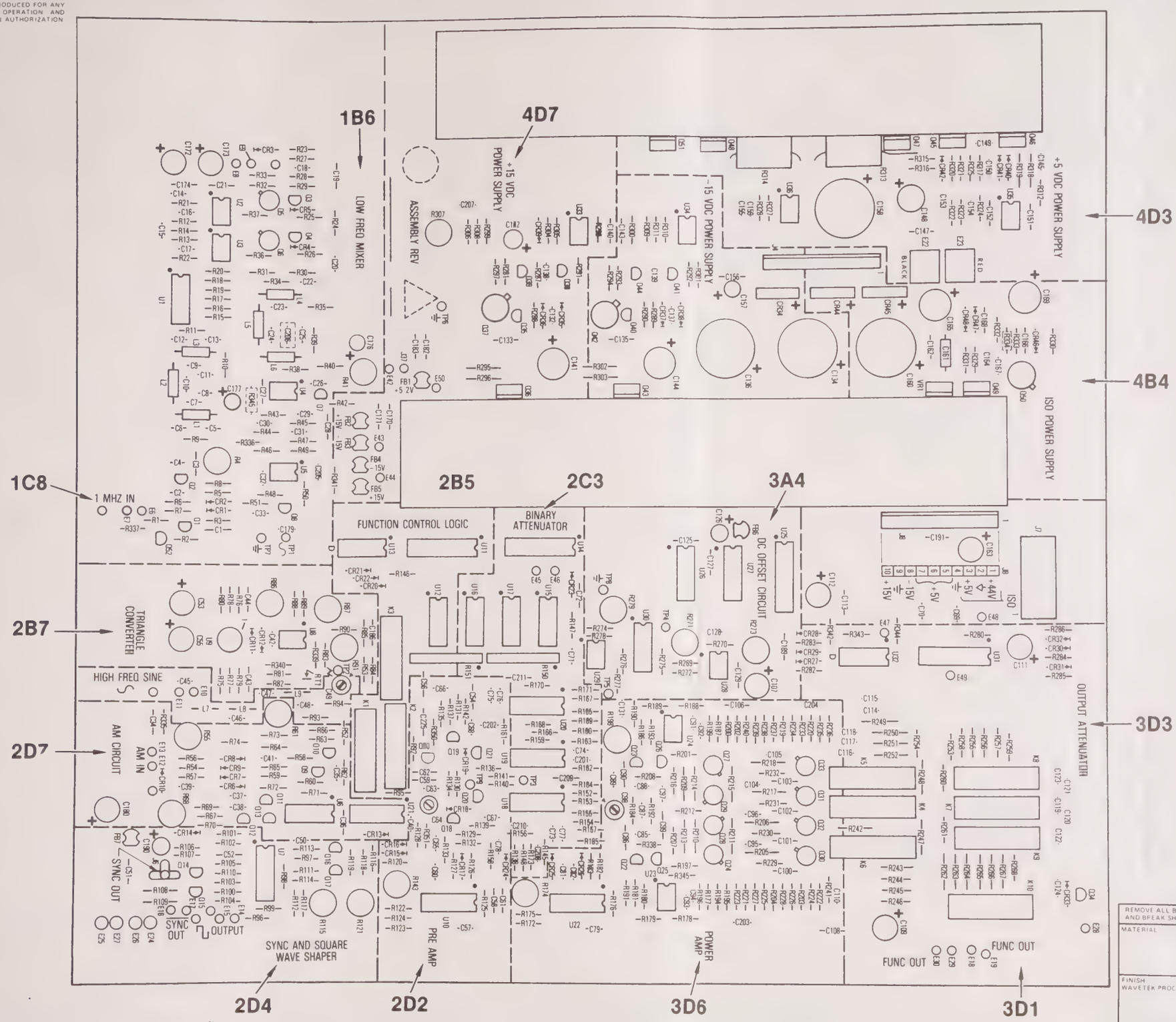
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN L. CHERMACK	DATE 5-5-80	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC OUTPUT/POWER SUPPLY BD. (A4)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 178	DWG NO 0103-00-0752 REV AE
		CODE IDENT 23338	SHEET 4 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3094

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REFERENCE KEY: 2D3

SCHEMATIC SHEET NO.
VERTICAL COORDINATE
HORIZONTAL COORDINATE



MADE FROM 0100-00-0752-3L

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA OUTPUT/POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ± 1 XX .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-0752 REV
	SCALE	CODE IDENT 23338	SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFOR MATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, OUTPUT/P. S	0101-00-0752	WVTK	0101-00-0752	1
NONE	SCHEMATIC, OUTPUT/P. S	0103-00-0752	WVTK	0103-00-0752	1
NONE	ASSY, WIRE 178-0928	178-2602	WVTK	1207-00-2602	1
NONE	KIT, PRE WAVE LOAD 178-0752	178-1308	WVTK	1208-00-1308	1
NONE	HEATSINK, MOD FROM: 2800-11-0011	166-8879	WVTK	1400-00-8879	1
NONE	SHIELD PARTITION	178-0201	WVTK	1400-01-0201	2
NONE	CORNER POST T REF: 3200-02-0004	178-0231	WVTK	1400-01-0231	1
NONE	HEATSINK REF: 3200-02-0006	178-0241	WVTK	1400-01-0241	1
NONE	HEATSINK REF: 3200-02-0006	178-0251	WVTK	1400-01-0251	1
NONE	SHIELD PARTITION	178-1291	WVTK	1400-01-1291	2
NONE	CORNER POST(X) REF: 3200-02-0004	178-1311	WVTK	1400-01-1311	3
NONE	HEATSINK, MOD FROM: 2800-11-0011	178-3129	WVTK	1400-01-3129	2
NONE	PLATE, LINKING	178-6241	WVTK	1400-01-6241	1

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT/P. S. | ASSEMBLY NO. 1100-00-0752 | REV AK

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	INSULATOR, MICA	64-21-023-106	ASHVL	3100-00-0006	9
R359	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R352 R355	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	2
R163	RES, MF, 1/8W, 1%, 4.12K	RN55D-4121F	TRW	4701-03-4121	1
R356	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R162	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
R313 R314	RES, WW, 10W, 3%, .1 OHM	RH10- 1 OHM 3%	DALE	4702-77-0019	2
Q36 Q46 Q49	TRANS, POWER, NPN, TO-220	2N6486	MOT	4901-06-4860	3
Q43 Q45 Q47 Q48	TRANS, POWER, PNP, TO-220	2N6489	MOT	4901-06-4890	4
Q51	TRANS, POWER, PNP, TO-220	2N6504	MOT	4901-06-5040	1
Q5 Q6	SWITCH, DMOS-FET, N-CHAN, ENHANCE MODE	BSD214	PHLP	4902-00-2140	2
Q26 Q27	TRANS	A-400	AMPRX	4902-00-4000	2
Q21 Q25	TRANS	A-440	AMPRX	4902-00-4400	2
RT1	THERMISTER, 10,0000HMS ,25%, CUST, COATED	155-180FAK-B01	FENWL	5300-00-0002	1

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT/P. S. | ASSEMBLY NO. 1100-00-0752 | REV AK

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, OUTPUT/P. S	0101-00-0752	WVTK	0101-00-0752	1
NONE	SCHEMATIC, OUTPUT/P. S	0103-00-0752	WVTK	0103-00-0752	1
NONE	PC BD, PREPPED 178-0752	178-1309	WVTK	1208-00-1309	1
C110T C200 C89 C97T	CAP, CER DISK, 5PF, 1KV, 10%	0311-00018	WVTK	1500-00-5011	4
C128	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C18 C203 C204 C67 C68	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	5
C149 C150 C159 C164 C167 C208 C26 C81	CAP, CER, .001UF, 1KV	DD-102	CRL	1500-01-0211	8
C104 C105 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C131 C132 C137 C14 C154 C155 C16 C17 C179 C20 C201 C202 C209 C211 C33 C39 C4 C41 C50 C65 C66 C71 C73 C74 C75 C76 C85 C87 C88 C95 C96	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	44
C1 C100 C101 C102 C103 C106 C108 C113 C125 C127 C129 C133 C135 C140 C143 C147 C151 C152 C156 C162 C166 C168 C170 C171 C174 C182 C183 C186 C189 C19 C191 C21 C225 C27 C28 C3 C34 C36 C43	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	51

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C242 NONE	CAP, CER DISK, 5PF, 1KV, 10%	0311-00018	WVTK	1500-00-5011	2
NONE	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	1
C245	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	1
NONE	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	1
C241	CAP, MICA, 120PF, 500V, RADIAL	DM15-121J	ARCO	1500-11-2100	1
C243	CAP, MICA, 150PF, 500V	DM15-151J	ARCO	1500-11-5100	1
C244	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
J6	CONN, COAX SOCKET	226287-2	AMP	2100-03-0038	1
NONE	SPRING SOCKET	50935-1	AMP	2100-03-0039	1
E22 E23	TERMINAL TAB (FASTON)	62747-1	AMP	2100-04-0038	2
NONE	SUPER KIT	2500-0178-01	WVTK	2500-0178-01	1
NONE	HEATSINK	26068H5E	WAKE	2800-11-0012	6
NONE	WASHER	5607-150	SESTM	2800-11-0015	9
NONE	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	4
NONE	BALUN CORE	2873000902	FARIT	3100-00-0002	5

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT/P. S. | ASSEMBLY NO. 1100-00-0752 | REV AK

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J7	ASSY, RIBBON CABLE 20 PIN X 5 LONG	6002-00-0014	WVTK	6002-00-0014	1
VR1	VOLT REGULATOR	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT/P. S. | ASSEMBLY NO. 1100-00-0752 | REV AK

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C44 C51 C52 C54 C56 C58 C59 C61 C62 C72 C86 C90					
C35	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	1
C40 C60	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	2
C145 C205 C207	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	3
C138 C139 C15 C63	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	4
C91	CAP, CER, 390PF, 1KV	DD-391	CRL	1500-03-9101	1
C82 C92 C93 C94	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	4
C79	CAP, CER, 560PF, 1KV	DD-561SLL	CRL	1500-05-6101	1
C69 C70	CAP, CER, 820PF, 1KV	DD-821 LONG LEAD	CRL	1500-08-2101	2
C37 C38 C46 C47	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	4
C48 C6	CAP, MICA, 15PF, 500V	DM15-150J	ARCO	1500-11-5000	2
C2	CAP, MICA, 150PF, 500V	DM15-151F	ARCO	1500-11-5101	1
C77	CAP, MICA, 20PF, 500V, RADIAL	DM15-200J	ARCO	1500-12-0000	1
C22 C30	CAP, MICA, 270PF, 500V	DM15-271J	ARCO	1500-12-7100	2
C42T	CAP, MICA, 30PF, 500V, RADIAL	DM15-300J	ARCO	1500-13-0000	1

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, OUTPUT/P.S.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-0752 REV AK
	SCALE	CODE IDENT 23338	SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3984

REV	ECN	BY	DATE	APP

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C13 C5	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C12 C206	CAP, MICA, 43PF, 500V	DM15-430J	ARCO	1500-14-3000	2
C7 C9	CAP, MICA, 47PF, 500V	DM15-470J	ARCO	1500-14-7000	2
C240	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	1
C10	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	1
C11 C8	CAP, MICA, 560PF, 300V	DM15-561J	ARCO	1500-15-6100	2
C23 C24 C25	CAP, MICA, 620PF, 300V 1%	CD15-621F	CDE	1500-16-2100	3
C45	CAP, MICA, 82PF, 500V	DM15-820J	ARCO	1500-18-2000	1
C107 C109 C111 C163 C172 C173 C53 C55	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	8
C112 C148 C180	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	3
C142	CAP, ELECT, 33MF, 25V RADIAL LEAD, SP .14	RLR 336RLR025M	IC	1500-33-3002	1
C141 C144 C165 C169	CAP, ELECT, 470MF/50V RADIAL LEAD, SP .30	CRE SERIES 470/50	CAPAR	1500-34-7103	4
C134 C136	CAP, ELECT, 4700MF/25V RADIAL LEAD, SP .50	NRE472M25V22X41	NIC	1500-34-7202	2
C158 C160	CAP, ELECT, 6800MF, 16V	NRE682M16V22X41-0.5LS	NIC	1500-36-8201	2

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	RADIAL LEAD, SP .50				
C99	CAP, MYLAR, .022MF100V	225P22391WD3	SPRAG	1500-42-2314	1
C64 C98	CAP, VAR, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	2
C49	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	1
C161	CAP, TANT, 1MF, 35V	150D105X9035A2	SPRAG	1500-71-0502	1
C126 C153 C157 C176 C177 C190	CAP, TANT, 22MF, 20V	202A2002226M3	MATSO	1500-72-2621	6
L1 L2 L3	CHOKE, 82MH, 5%	1537-72	DLVAN	1800-00-0005	3
L7 L9	CHOKE, .18MH, 10%	1025-02	DLVAN	1800-00-0012	2
L8	INDUCTOR, .22 MICRO H	1025-04	DELVN	1800-00-0021	1
L10	INDUCTOR, 330MH	2500-04	DELVN	1800-00-0022	1
L5 L6	INDUCTOR, 390MH	2500-08	DELVN	1800-00-0023	2
J4 J8	CONN, HEADER	1-640386-0	AMP	2100-02-0079	2
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	9
NONE	TRANSIPAD	10123N	METRS	2800-11-0003	11
NONE	BALUN CORE	2873000902	FARIT	3100-00-0002	2

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
K1 K2 K3 K5 K6 K7 K8 K9	RELAY, REED, FORM-A	1503-10-3	WABSH	4500-00-0007	8
K10 K4	RELAY, REED, FORM-C	RA30571051	ETROL	4500-00-0009	2
R271 R41 R86	POT, TOP TRIM, 20T, 100K	68WR100K	BECK	4609-90-0001	3
R279	POT, TOP TRIM, 20T, 10K	68WR10K	BECK	4609-90-0002	1
R115 R307 R4 R55 R61	POT, TOP TRIM, 20T, 1K	68WR1K	BECK	4609-90-0005	5
R143 R174 R198 R68 R91	POT, TOP TRIM, 20T, 100	68WR100	BECK	4609-90-0019	5
R273 R87	POT, TOP TRIM, 20T, 200	68WR200	BECK	4609-90-0020	2
R121	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	1
R318 R319	RES, C, 1/2W, 5%, 10	RC-1/2-100J	STKPL	4700-25-0100	2
R295 R296 R302 R303	RES, C, 1/2W, 5%, 1.8	RC-1/2-1R8J	STKPL	4700-25-0189	4
R205 R206 R217 R218	RES, C, 1/2W, 5%, 27	RC-1/2-270J	STKPL	4700-25-0270	4
R1 R11 R127 R14 R182 R305 R336 R51 R66 R7 R82	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	11
R158 R161 R17 R25 R26 R281 R286 R291 R292 R293 R298 R301 R317 R320 R353 R354 R49 R74 R89	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	19
R168 R184 R21 R22 R287 R289	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	6

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R358	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R133 R140 R141 R229 R230 R231 R232 R282 R283 R284 R285 R59 R65	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	13
R101 R147 R30 R50 R71	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	5
R299 R300	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	2
R253 R254 R81	RES, MF, 1/8W, 1%, 124	RN55D-1240F	TRW	4701-03-1240	3
R126 R195 R202 R72 R98	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	5
R12 R13	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2
R138 R15 R177 R178 R187 R188 R19 R270 R32 R33 R332 R64	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	12
R134 R53	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	2
R77 R78	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	2
R119 R197 R201 R212 R288 R290 R36 R37 R52 R83 R90 R92 R94	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	13
R280 R340 R342 R343 R344 R58	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	6
R170	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	1

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 6

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R207 R216 R221 R222 R223 R224 R225 R226 R227 R228 R233 R234 R235 R236 R237 R238 R239 R240 R331 R339 R69 R84 R95	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	23
R304	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R122 R128 R139 R142 R159 R260 R261 R357	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	8
R120 R16 R165 R18 R259 R27 R57 R73	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	8
R192 R337 R62	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	3
R67	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R118 R277T R3 R345 R8	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	5
R79 R80	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	2
R269 R40 R88	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	3
R106 R107	RES, MF, 1/8W, 1%, 30.1	RN55D-30R1F	TRW	4701-03-3019	2
R70	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	1
R123 R124 R125 R172 R175 R176 R350	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	7
R75 R76	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R105 R110 R111 R114 R312 R315 R316	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	7
R333 R54	RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	2
R56	RES, MF, 1/8W, 1%, 3.74K	RN55D-3741F	TRW	4701-03-3741	1
R132 R185 R9	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	3
R23 R60 R63	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	3
R24	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R5	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	1
R10 R102 R103 R104 R112 R117 R135 R173 R191 R20 R294 R297 R321 R351 R42 R47 R99	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	17
R116 R129 R131 R146 R167 R180 R190 R194 R196 R199 R2 R200 R272 R275 R276 R28 R309 R31 R328	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	19
R108 R109 R341	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	3
R160 R203 R204 R219 R220 R327	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	6
R136 R34 R6 R85	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	4
R241 R93	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	2

WAVETEK PARTS LIST | TITLE: KIT, PRE WAVE LOAD 178-0752 | ASSEMBLY NO. 1208-00-1308 | REV AE | PAGE 8

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, OUTPUT/P.S.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 178 / DWG NO. 1100-00-0752 / REV AK
	SCALE		CODE IDENT 23338 / SHEET 2 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R308	RES, MF, 1/8W, 1%, 7.15K	RN55D-7151F	TRW	4701-03-7151	1
R100 R193 R208 R329 R335 R338 R97	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	7
R130 R179 R181 R186 R189 R325 R330	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	7
R29 R346	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	2
R322	RES, MF, 1/8W, 1%, 8.87K	RN55D-8871F	TRW	4701-03-8871	1
R163	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1
R166	RES, MF, 1/8W, 1%, 976	RN55D-9760F	TRW	4701-03-9760	1
R306	RES, MF, 1/8W, 1%, 9.76K	RN55D-9761F	TRW	4701-03-9761	1
R243 R244	RES, MF, 1/4W, 1%, 100	RN60D-1000F	TRW	4701-13-1000	2
R245 R246 R249 R250	RES, MF, 1/4W, 1%, 121	RN60D-1210F	TRW	4701-13-1210	4
R247 R248 R251 R252	RES, MF, 1/4W, 1%, 124	RN60D-1240F	TRW	4701-13-1240	4
R258	RES, MF, 1/4W, 1%, 196	RN60D-1960F	TRW	4701-13-1960	1
R253 R256 R257 R262 R263 R264 R265 R266 R267	RES, MF, 1/4W, 1%, 332	RN60D-3320F	TRW	4701-13-3320	9
R209 R210 R211 R213 R214 R215 R242	RES, MF, 1/4W, 1%, 49.9	RN60D-49R9F	TRW	4701-13-4999	7

WAVETEK PARTS LIST	TITLE KIT, PRE WAVE LOAD 178-0752	ASSEMBLY NO. 1208-00-1308	REV AE
		PAGE 9	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
CR41 CR47 CR48					
CR6 7 8 9	DIODE, SET, 4-FD-6666 QTY: 4: 4807-02-6666	4898-00-0013	WVTK	4898-00-0013	1
Q27 Q37	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	2
Q1	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	1
Q24 Q42	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	2
Q19 Q23 Q3 Q4	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	4
Q38 Q39 Q40	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3642	FAIR	4901-03-6420	3
Q34 Q7	TRANS, NPN, -TO-92	MPS3646	MOT	4901-03-6460	2
Q50	TRANS, NPN, TO-39	2N3725	FAIR	4901-03-7250	1
Q28 Q31 Q33	TRANS	2N3866	MOT	4901-03-8660	3
Q2	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3903	NSC	4901-03-9030	1
Q60	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906	FAIR	4901-03-9060	1
Q35 Q41 Q44	TRANS, LOW LEVEL, PNP, TO-92	2N4248	FAIR	4901-04-2480	3

WAVETEK PARTS LIST	TITLE KIT, PRE WAVE LOAD 178-0752	ASSEMBLY NO. 1208-00-1308	REV AE
		PAGE 11	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R113	RES, MF, 1/4W, 1%, 71.5	RN60D-71R5F	TRW	4701-13-7159	1
R150 R151	RES NETWORK 22K 2% 10PIN SIP BUSS	4310R-101-223	BOURN	4770-00-0033	2
R274 278 R310 311 R323 324	RES, SET, 2-10K, 1/8W QTY: 2: 4701-03-1002	4789-00-0019	IRC	4789-00-0019	3
R152 153 154 155 156 157	RES, SET, 6-1.5K, 1/8W QTY: 6: 4701-03-1501	4789-00-0047	WVTK	4789-00-0047	1
R345 R44 R46 R48	RES, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	4
CR40 CR42	DIODE, ZENER, 3.3V, 5% TOL, 500MW, G/B, IN746A	1N746A	FAIR	4801-01-0746	2
CR10 CR39 CR46	DIODE, REFERENCE, LOW LEVEL, TEMP COMP	1N4581	MICRO	4801-01-4581	3
CR23	DIODE, ZENER 9.1V, GLASS SILICON, 500MW	1N5239	TEL	4801-01-5239	1
CR34 CR44 CR45	DIODE, RECTIFIER, BRIDGE	3N255	GI	4801-02-0254	3
CR15 CR16 CR4 CR5	DIODE, ULTRA FAST	1N4244	T/CBF	4807-02-0777	4
CR1 CR11 CR12 CR13 CR14 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR26 CR27 CR28 CR29 CR3 CR30 CR31 CR32 CR33 CR35 CR36 CR37 CR38	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	28

WAVETEK PARTS LIST	TITLE KIT, PRE WAVE LOAD 178-0752	ASSEMBLY NO. 1208-00-1308	REV AE
		PAGE 10	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
Q8	TRANS, GENERAL PURPOSE, PNP, TO-92	2N5139	FAIR	4901-05-1390	1
Q30 Q32	TRANS	2N5160-18	MOT	4901-05-1600	2
Q52	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	1
Q29	TRANS 2N5583 PNP HIGH FREQ TO-39	2N5583	MOT	4901-05-5830	1
Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q22 Q9	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	11
U30	SWITCH, DUAL COMPLEMENTARY SPST	TL188CN	TI	7000-01-8800	1
U2 U3 U8	OP AMP, HIGH SPEED	LM318H	AMD	7000-03-1800	3
U12 U15 U16 U17	COMPARATORS, QUAD VOLTAGE	0665-00364	WVTK	7000-03-3900	4
U5	OP AMP	LF357N	NSC	7000-03-5700	1
U27	DAC, MONOLITHIC, 10 BIT	AD 561 J	AD	7000-05-6100	1
U23 U24 U28 U29 U33 U34 U35	OP AMP, INTERNALLY COMP, HIGH PERFORMANCE	LM741CN	NSC	7000-07-4100	7
U6	MODULATOR-DEMODULATOR, BALANCED	MC1496P	MOT	7000-14-9600	1

WAVETEK PARTS LIST	TITLE KIT, PRE WAVE LOAD 178-0752	ASSEMBLY NO. 1208-00-1308	REV AE
		PAGE 12	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U9	DIODE, ULTRA FAST, LOW CAPACITANCE	CA-3019	RCA	7000-30-1900	1
U1	TRANS ARRAY, GENERAL PURPOSE NPN	CA-3046	RCA	7000-30-4600	1
U10 U22	TRANS ARRAY, NPN/PNP	CA-3096AE	RCA	7000-30-9600	2
U36	SENSING CIRCUIT, OVERVOLTAGE	MC 3423	MOT	7000-34-2300	1
U18 U19 U20 U21	ANALOG SWITCH ARRAY, DMOS FET QUAD	SD5000N	SIG	7000-50-0000	4
U13 U32	INVERTER BUFRS/DRVRS, HEX, W/OC HIGH VOLT O/P	7416	SIG	8000-74-1600	2
U7	GATE XOR/XNOR, TRI 2 INP, ECL	MC10107	MOT	8001-01-0700	1
U26	FLIP-FLOP, QUAD D, TTL	74LS175	TI	8007-41-7510	1
U11 U14 U25	FLIP-FLOP, OCT D, TTL	74LS273	TI	8007-42-7310	3
U31	FLIP-FLOP, OCT D, TTL	74LS374	TI	8007-43-7410	1

WAVETEK PARTS LIST	TITLE KIT, PRE WAVE LOAD 178-0752	ASSEMBLY NO. 1208-00-1308	REV AE
		PAGE 13	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, OUTPUT/P.S.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 1100-00-0752 REV AK
	SCALE	CODE IDENT 23338	SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3864

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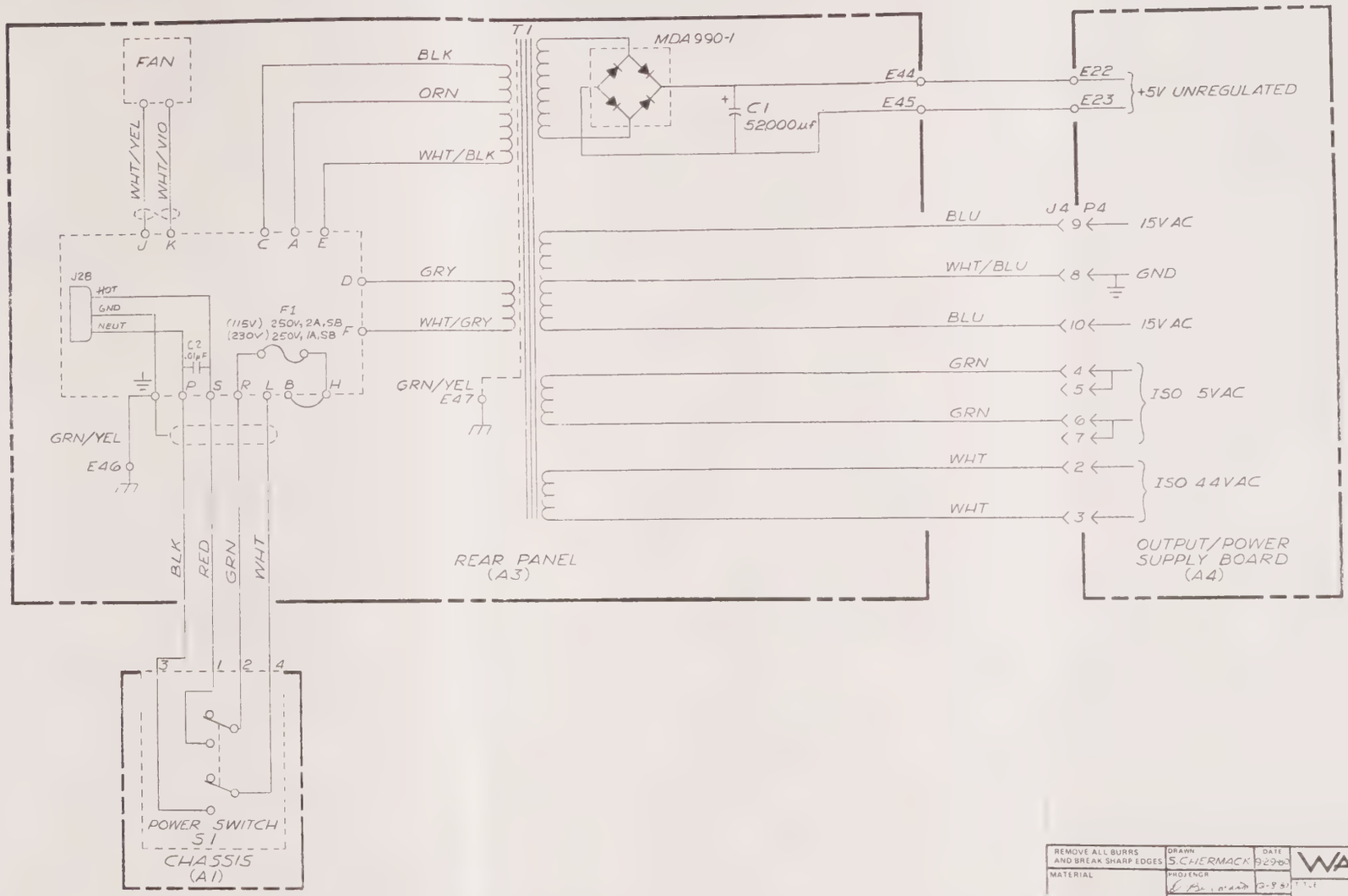
REV	ECN	BY	DATE	APP



1. PARTIAL REAR PANEL REFERENCE DESIGNATORS SHOWN, PREFIX WITH ASSEMBLY REF DES (A3)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 9-29-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR	10-8-83	TITLE: SCHEMATIC: REAR PANEL (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV		TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
	DO NOT SCALE DWG		MODEL NO 178
	SCALE		DWG NO 0103-00-0814 REV
	CODE IDENT 23338		SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RED IDER NO A-3864

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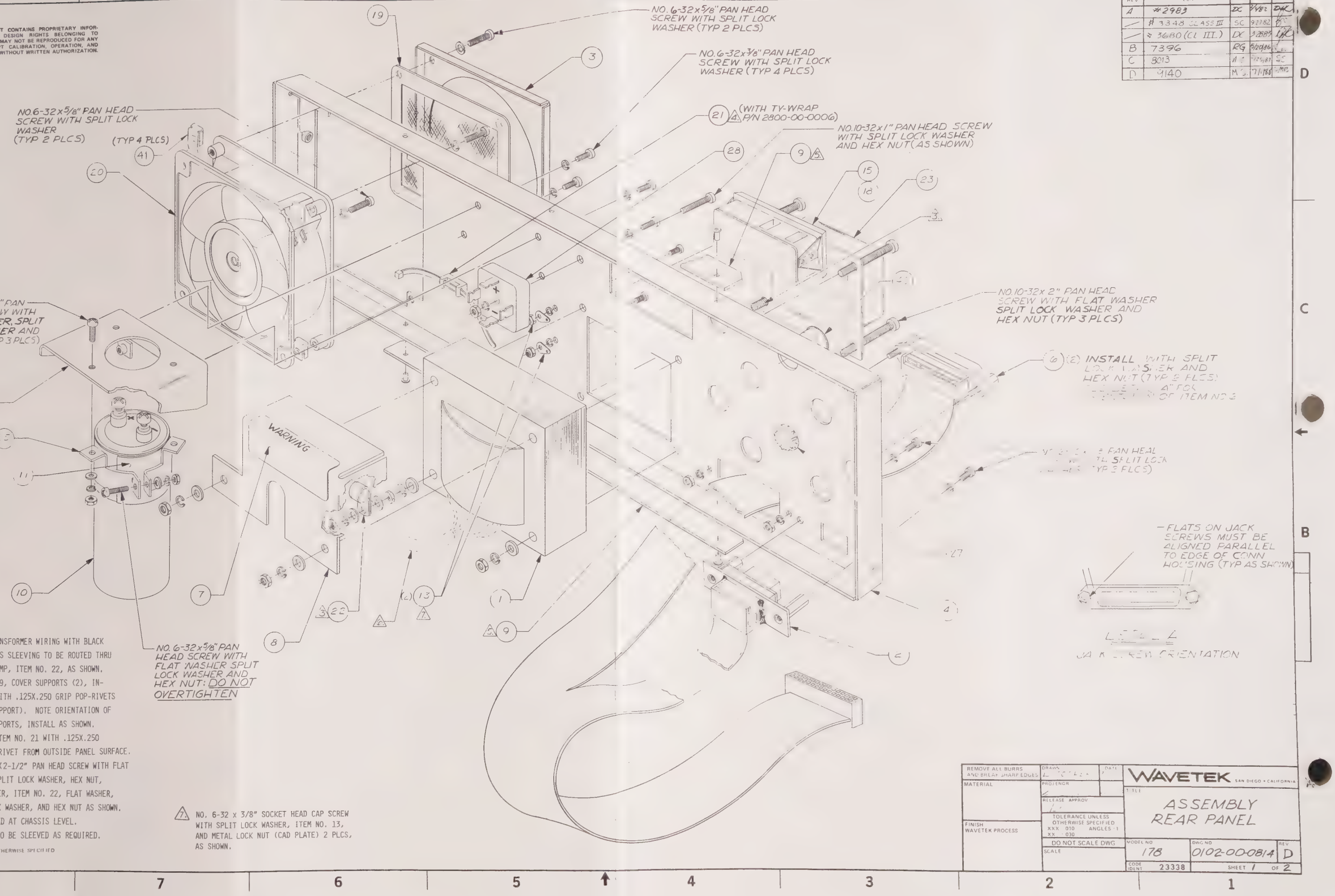
REV	ECN	BY	DATE	APP
A	#2983	DC	8/4/82	DMK
/	# 3348 CLASS III	SC	9/21/82	
/	# 3680 (CL III.)	DC	3/28/83	DMK
B	7396	RG	5/20/86	
C	8013	M	4/25/87	SC
D	9140	M	7/1/88	MD


NO. 6-32x5/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (TYP 2 PLCS)
NO. 6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (TYP 4 PLCS)
NO. 6-32x5/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (TYP 2 PLCS)
(TYP 4 PLCS)
(WITH TY-WRAP P/N 2800-00-0006)
NO. 10-32x1" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND HEX NUT (AS SHOWN)
NO. 6-32x3/8" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT (TYP 3 PLCS)
NO. 10-32x 2" PAN HEAD SCREW WITH FLAT WASHER SPLIT LOCK WASHER AND HEX NUT (TYP 3 PLCS)
INSTALL WITH SPLIT LOCK WASHER AND HEX NUT (TYP 3 PLCS)
WARNING
NO. 6-32x5/8" PAN HEAD SCREW WITH FLAT WASHER SPLIT LOCK WASHER AND HEX NUT: DO NOT OVERTIGHTEN
FLATS ON JACK SCREWS MUST BE ALIGNED PARALLEL TO EDGE OF CONN HOUSING (TYP AS SHOWN)
JACK SCREW ORIENTATION

6. (REF) TRANSFORMER WIRING WITH BLACK FIBERGLASS SLEEVING TO BE ROUTED THRU CABLE CLAMP, ITEM NO. 22, AS SHOWN.
5. ITEM NO. 9, COVER SUPPORTS (2), INSTALLED WITH .125X.250 GRIP POP-RIVETS (3 PER SUPPORT). NOTE ORIENTATION OF COVER SUPPORTS, INSTALL AS SHOWN.
4. INSTALL ITEM NO. 21 WITH .125X.250 GRIP POP-RIVET FROM OUTSIDE PANEL SURFACE.
3. NO. 10-32X2-1/2" PAN HEAD SCREW WITH FLAT WASHER, SPLIT LOCK WASHER, HEX NUT, FLAT WASHER, ITEM NO. 22, FLAT WASHER, SPLIT LOCK WASHER, AND HEX NUT AS SHOWN.
2. TO BE WIRED AT CHASSIS LEVEL.
1. ALL WIRE TO BE SLEEVED AS REQUIRED.

NOTE UNLESS OTHERWISE SPECIFIED

7. NO. 6-32 x 3/8" SOCKET HEAD CAP SCREW WITH SPLIT LOCK WASHER, ITEM NO. 13, AND METAL LOCK NUT (CAD PLATE) 2 PLCS, AS SHOWN.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 178	DWG NO 0102-00-00814 REV D
		CODE IDENT 23338	SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS MI ORDER NO A 3894

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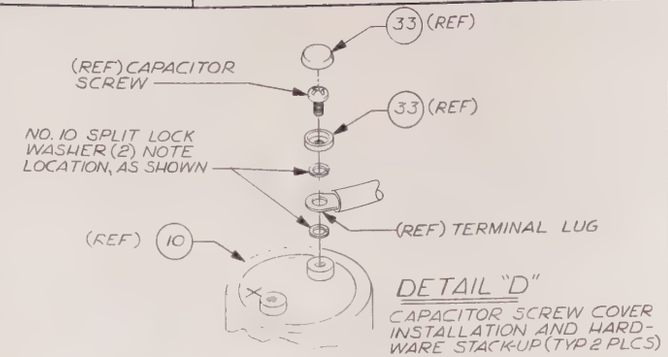
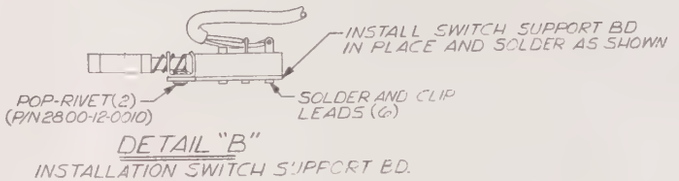
REV	ECN	BY	DATE	APP

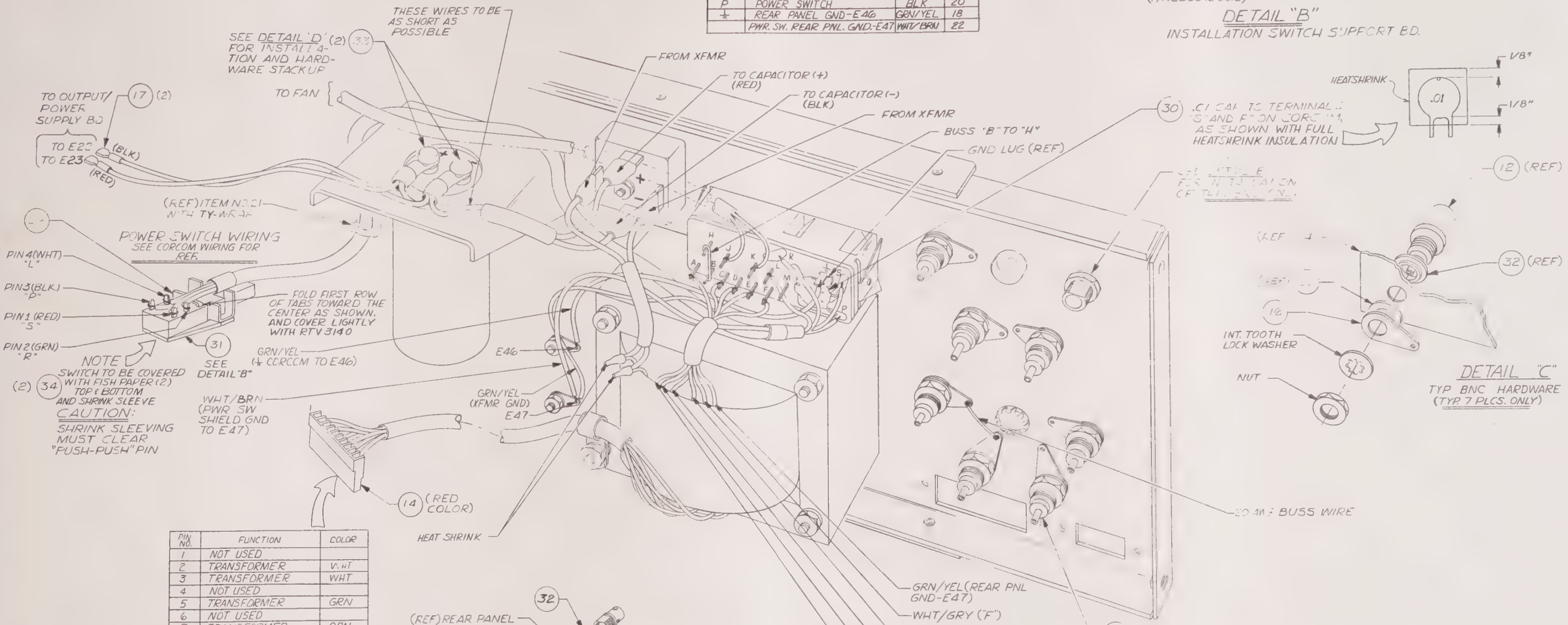


DETAIL "D"
CAPACITOR SCREW COVER INSTALLATION AND HARDWARE STACK-UP (TYP 2 PLCS)

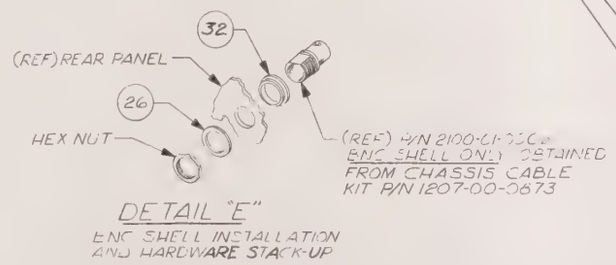
CORCOM WIRING			
PIN NO.	DESTINATION	COLOR	GA.
A	TRANSFORMER	ORN	24
B	JUMPER TO "H"		
C	TRANSFORMER	BLK	24
D	TRANSFORMER	GRY	24
E	TRANSFORMER	WHT/BLK	24
F	TRANSFORMER	WHT/GRY	24
H	JUMPER TO "B"		
J	FAN	WHT/YEL	22
K	FAN	WHT/VIO	22
L	POWER SWITCH	WHT	20
M	NOT USED		
R	POWER SWITCH	GRN	20
S	POWER SWITCH	RED	20
P	POWER SWITCH	BLK	20
⏚	REAR PANEL GND-E46	GRN/YEL	18
	PWR. SW. REAR PNL. GND.-E47	WHT/BRN	22



DETAIL "B"
INSTALLATION SWITCH SUPPORT BD.



PIN NO.	FUNCTION	COLOR
1	NOT USED	
2	TRANSFORMER	V. HT
3	TRANSFORMER	WHT
4	NOT USED	
5	TRANSFORMER	GRN
6	NOT USED	
7	TRANSFORMER	GRN
8	TRANSFORMER	WHT/BLU
9	TRANSFORMER	BLU
10	TRANSFORMER	BLU



DETAIL "E"
BNC SHELL INSTALLATION AND HARDWARE STACK-UP

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D COOPER	DATE 7-7-87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	ENGR		TITLE ASSEMBLY REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0102-00-0814 REV D
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0814	WVTK	0102-00-0814	1
NONE	SCHEMATIC, REAR PANEL	0103-00-0814	WVTK	0103-00-0814	1
1	TRANSFORMER, POWER	178-0032	WVTK	1204-00-0032	1
2	ASSY, GPIB DECODER	178-0865	WVTK	1208-00-0865	1
3	SCREEN COVER	172-7523	WVTK	1400-00-7523	1
34	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	2
NONE	LABEL, OPTION	172-8880	WVTK	1400-00-8880	1
NONE	END BELL, CHROME	1400-00-9014	WVTK	1400-00-9014	1
4	PANEL, REAR	178-0150	WVTK	1400-01-0150	1
5	BRACKET, CAPACITOR	178-0163	WVTK	1400-01-0163	1
6	JACK SCREW	859-0530	WVTK	1400-01-0530	2
7	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
8	SHIELD, H.V.	178-1633	WVTK	1400-01-1633	1
9	COVER SUPPORT	178-2033	WVTK	1400-01-2033	2
11	POLYESTER FILM REF: 1600-99-0002	175-3191	WVTK	1400-01-3191	1
30	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	1

WAVETEK PARTS LIST | TITLE REAR PANEL | ASSEMBLY NO. 1101-00-0814 | REV U

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
10	CAP, ELEC, 52000MF, 15V	FAHM52000-15-B3	CDE	1500-35-2301	1
31	PCB, SWITCH SUPPORT BD REF SPEC 0008-00-0455 REV C	859-0750	WVTK	1700-00-0750	1
12	CONN BNC	KC-7946	KING	2100-01-0002	7
14	HOUSING	1-640433-0	AMP	2100-02-0080	1
15	CONN, RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
16	SOLDER LUG	1497	SMITH	2100-04-0012	7
NONE	LUG	35	ILSCO	2100-04-0018	2
13	SOLDER LUG	11A144	ZIER	2100-04-0025	2
17	TERMINAL RECEPTACLE (FASTON)	640919-2	AMP	2100-04-0039	2
18	FUSE, 2A, 250V, S-B	MDX 2	BUSS	2400-05-0030	1
19	FAN FILTER	5502	PAMOT	2600-01-0005	1
20	FAN, MODIFIED FROM 2600-00-0008	2600-99-0003	WVTK	2600-99-0003	1
21	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
22	CABLE CLAMP	770-1505	CONCD	2800-00-0010	1

WAVETEK PARTS LIST | TITLE REAR PANEL | ASSEMBLY NO. 1101-00-0814 | REV U

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
41	MOUNTING CLIP	512011	IMC	2800-09-0033	4
25	CAP, MTG, BAT	FJMR	STM	2800-12-0006	1
NONE	RIVET 3/32X3/16L	1131-0306	AVDEL	2800-12-0010	2
NONE	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	6
NONE	SCREW, 10-32 HEX NUT, Z	10-32 HEX NUT	CMRCL	2800-14-1000	4
NONE	SCREW, 10-32X2.5, PH, PH LP, NP	2800-18-0140	CMRCL	2800-18-0140	1
NONE	SCREW, 10-32X2, PHP, Z	10-32X2 PH	CMRCL	2800-18-0232	3
NONE	WASHER, FLAT, PLATED, #10	SAE 10	CMRCL	2800-26-0000	4
32	WASHER, SHOULDER, WHITE	2668	SMITH	2800-27-0004	8
26	WASHER NYLON FLAT	2264-N-385	AMTOM	2800-28-0005	8
33	SCREW COVER	12/12FLT BTM BLK 180	PRODC	2800-28-0012	2
27	PLUG BUTTON	2643/DP-500 BLACK	HEYCO	2800-35-0003	1
40	PLUG BUTTON	2663(BLACK)	HEYCO	2800-35-0004	1
NONE	#10 LOCKWASHER, PLATED	#10 REG	CMRCL	2800-42-0000	4
28	BRIDGE ASSY 30 AMP	MDA990-1	MOT	4899-00-0010	1
29	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST | TITLE REAR PANEL | ASSEMBLY NO. 1101-00-0814 | REV U

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 178 · DWG NO 1101-00-0814 · REV U
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894

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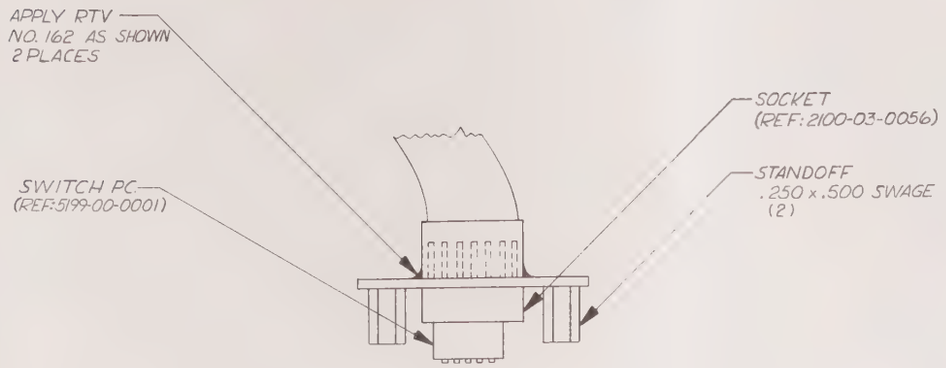
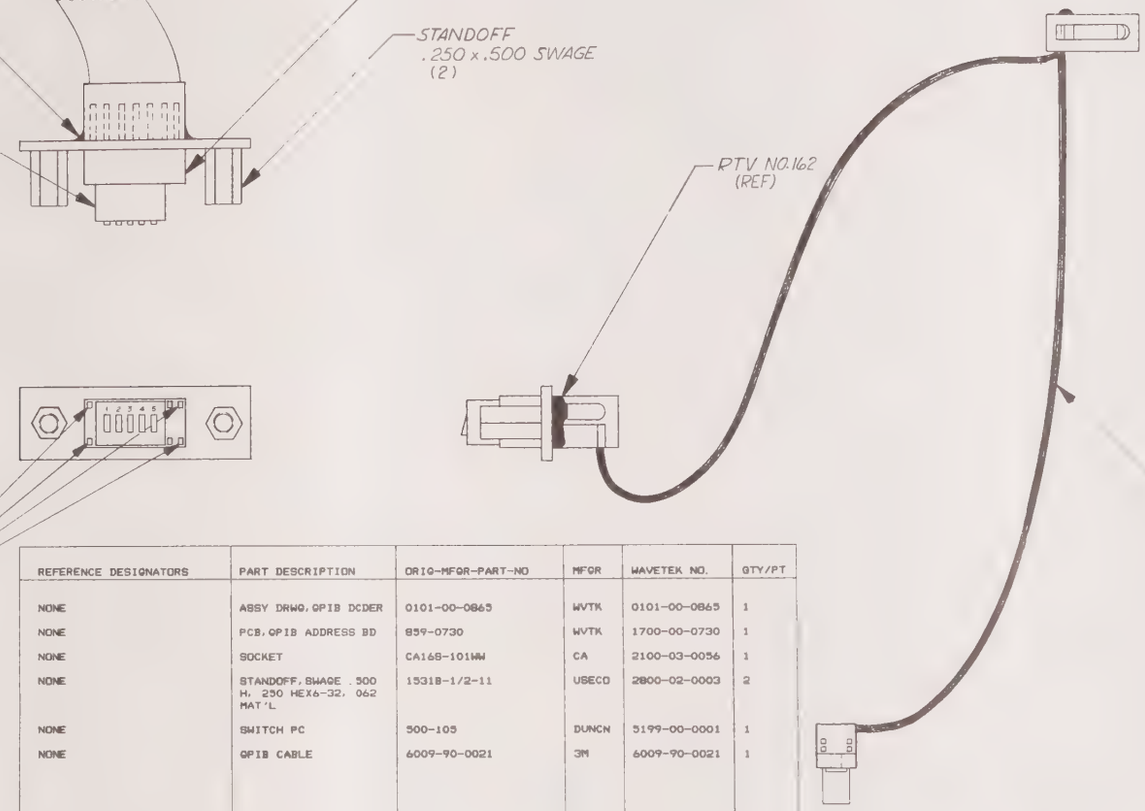
REV	ECN	BY	DATE	APP
A	2577	LDU	12/4/81	





SOLDER THESE FOUR PINS ONLY, PRIOR TO INSTALLING GPIB CABLE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, GPIB DCDER	0101-00-0865	WVTK	0101-00-0865	1
NONE	PCB, GPIB ADDRESS BD	859-0730	WVTK	1700-00-0730	1
NONE	SOCKET	CA16S-101WW	CA	2100-03-0056	1
NONE	STANDOFF, SWAGE .500 H, 250 HEX6-32, 062 MAT'L	1531B-1/2-11	USECO	2800-02-0003	2
NONE	SWITCH PC	500-105	DUNCN	5199-00-0001	1
NONE	GPIB CABLE	6009-90-0021	3M	6009-90-0021	1

WAVETEK PARTS LIST	TITLE: ASSY, GPIB DECODER	ASSEMBLY NO. 1208-00-0865	REV A

PAGE 1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: RO FIFER	DATE: 7/24/80	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY GPIB DECODER BD.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO: 178	DWG NO: 0101-00-0865 REV A
	SCALE: 1:1	CODE IDENT: 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A 3894

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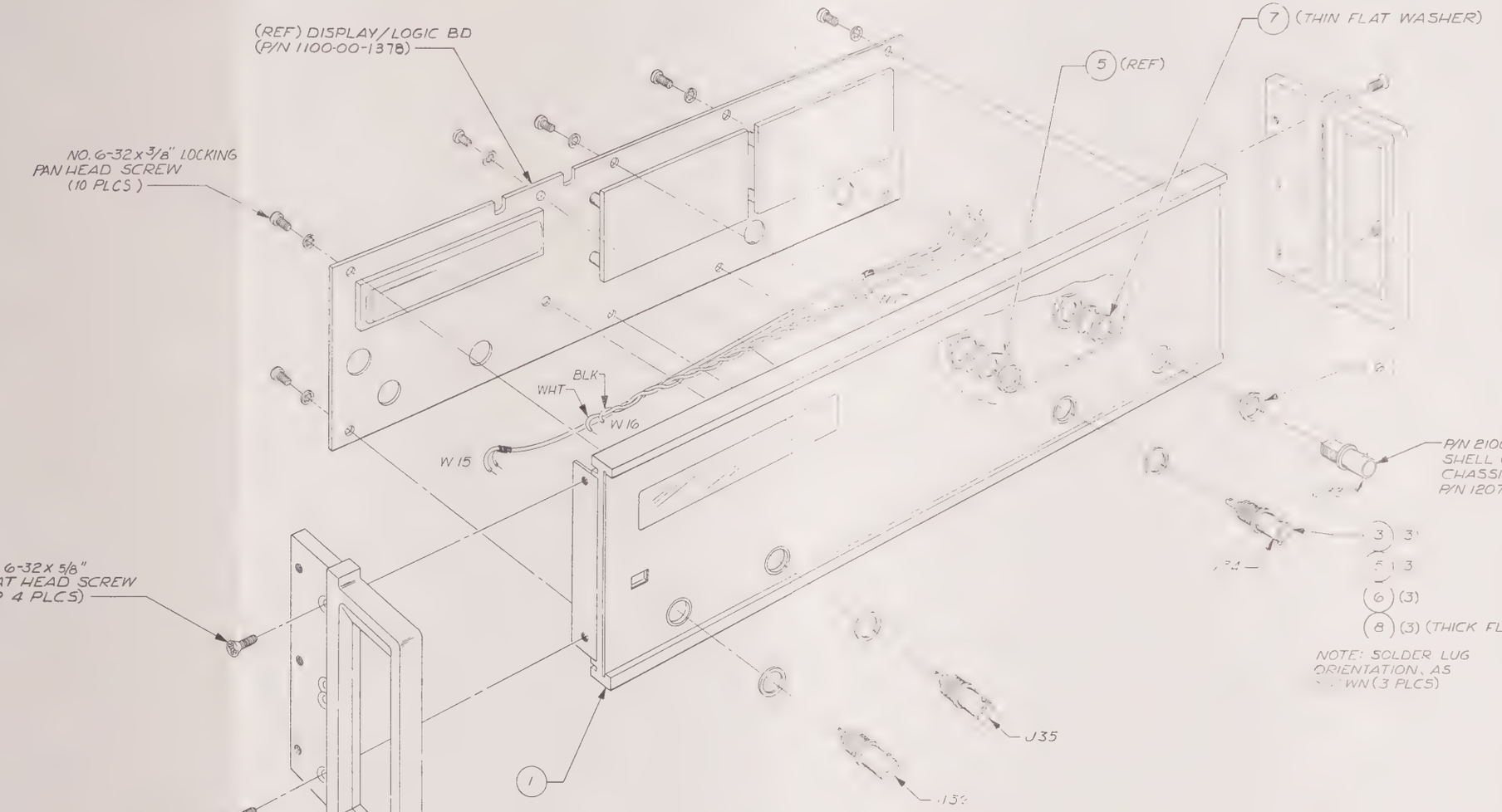
REV	ECN	BY	DATE	APP
A	ECN 4349	RO	9589	
B	ECN 4444	[illegible]	3-28-85	
C	ECO # 7884	[illegible]	1-9-87	S.S.
D	ECO # 7818	BR	4/3/87	



CABLE DESTINATION LIST

ALL CABLES OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-0873

CABLE#	FROM	TO	
W15	J36	J39	FREQ GEN
W16	J35	E33,E34	BOARD
W17	J34	J6	OUTPUT/PWR SUPPLY BD
NOTE: BLK WIRES ARE GND			

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-16-87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY FRONT PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0102-00-0892 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. FRONT PANEL	0102-00-0892	WVTK	0102-00-0892	1
NONE	DISPLAY, LOGIC BD	178-1378	WVTK	1100-00-1378	1
1	ASSY, SUB PANEL	178-0893	WVTK	1206-00-0893	1
NONE	SUPER KIT	2500-0178-03	WVTK	2500-0178-03	1
9	SCREW, PAN CAD I WITH LONGLOK 6-32 X 3/8	6-32X3/8 PAN LL	CMRCL	2800-23-6106	10
NONE	WASHER, 1/2 IN IT	1/2 IN IT WASHER	CMRCL	2800-24-0008	3

WAVETEK PARTS LIST	TITLE ASSY. FRONT PANEL	ASSEMBLY NO. 1101-00-0892	REV B
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, FRONT PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG.	MODEL NO. 178	DWG NO. 1101-00-0892 REV B
	SCALE	CODE IDENT. 23338	SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. A2088

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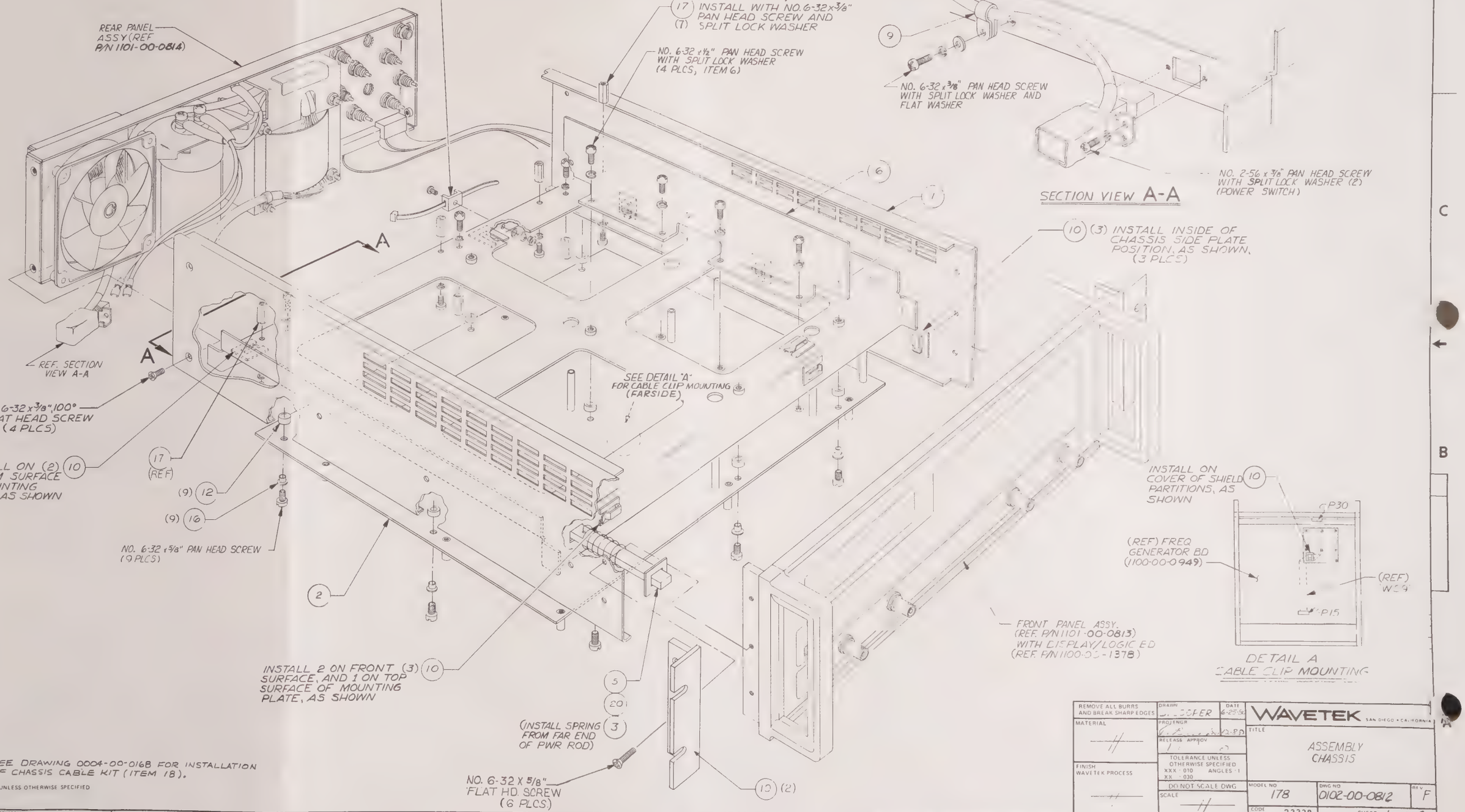
REV	ECN	BY	DATE	APP
A	ECN 2548	LOU	9/4/81	
B	4289 & 4305	SC	6/8/84	
C	4444 & 4716	SM	3/28/85	
D	7003	RO	2-17-86	
E	ECO # 7918		3/26/86	
F	ECO # 9141	MS	7/26/88	DMB


REAR PANEL ASSY (REF P/N 1101-00-0814)
8 WITH TY-WRAP (P/N 2800-00-0006) INSTALL WITH NO. 4-40 x 1/4" PAN HEAD SCREW, FLAT WASHER, SPLIT LOCK WASHER AND HEX NUT
(3/4" STANDOFF) 17 INSTALL WITH NO. 6-32 x 3/8" PAN HEAD SCREW AND (7) SPLIT LOCK WASHER
NO. 6-32 x 1/2" PAN HEAD SCREW WITH SPLIT LOCK WASHER (4 PLCS, ITEM 6)
9
NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND FLAT WASHER
NO. 2-56 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (2) (POWER SWITCH)
SECTION VIEW A-A
6
1
A
A
REF. SECTION VIEW A-A
NO. 6-32 x 3/8", 100° FLAT HEAD SCREW (4 PLCS)
INSTALL ON (2) 10 BOTTOM SURFACE OF MOUNTING PLATE, AS SHOWN
17 (REF)
(9) 12
(9) 16
NO. 6-32 x 5/8" PAN HEAD SCREW (9 PLCS)
SEE DETAIL "A" FOR CABLE CLIP MOUNTING (FARSIDE)
2
INSTALL 2 ON FRONT (3) 10 SURFACE, AND 1 ON TOP SURFACE OF MOUNTING PLATE, AS SHOWN
5
20
(INSTALL SPRING 3 FROM FAR END OF PWR ROD)
NO. 6-32 X 5/8" FLAT HD. SCREW (6 PLCS)
13 (2)
10 (3) INSTALL INSIDE OF CHASSIS SIDE PLATE POSITION, AS SHOWN. (3 PLCS)
INSTALL ON COVER OF SHIELD PARTITIONS, AS SHOWN
10
P30
(REF) FREQ GENERATOR BD (1100-00-0949)
(REF) W59
P15
DETAIL A CABLE CLIP MOUNTING
FRONT PANEL ASSY. (REF. P/N 1101-00-0813) WITH DISPLAY/LOGIC ED (REF. P/N 1100-00-1378)

1. SEE DRAWING 0004-00-0168 FOR INSTALLATION OF CHASSIS CABLE KIT (ITEM 18).

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN [illegible] DATE 6-25-86	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR [illegible]	TITLE	ASSEMBLY CHASSIS
FINISH WAVETEK PROCESS	RELEASE APPROV [illegible]	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0102-00-0812 REV F
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894

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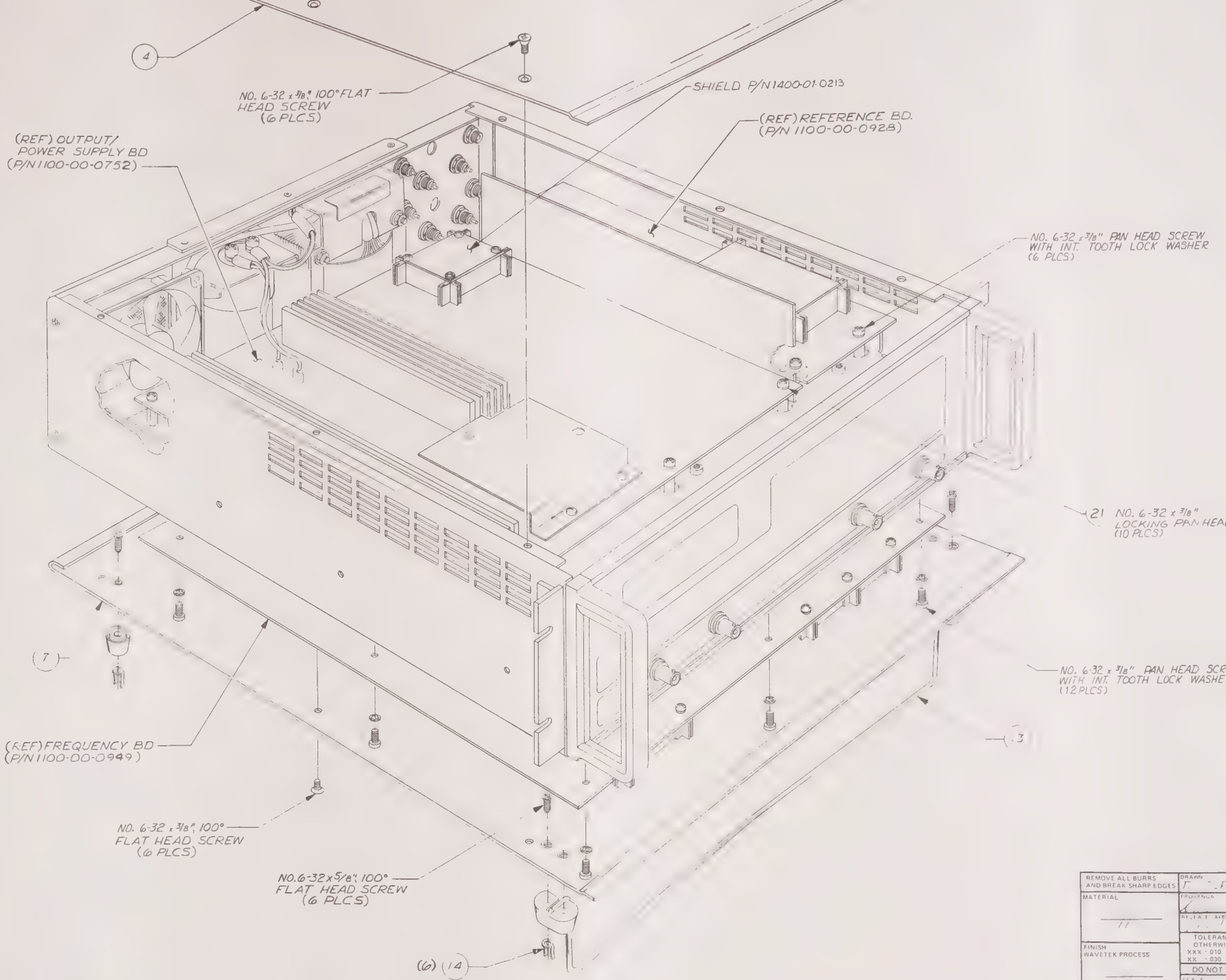
REV	ECN	BY	DATE	APP

SEE SHT. 1


4
NO. 6-32 x 3/8" 100° FLAT HEAD SCREW (6 PLCS)
SHIELD P/N 1400-01-0213
(REF) REFERENCE BD. (P/N 1100-00-0928)
(REF) OUTPUT/ POWER SUPPLY BD (P/N 1100-00-0752)
NO. 6-32 x 3/8" PAN HEAD SCREW WITH INT. TOOTH LOCK WASHER (6 PLCS)
21 NO. 6-32 x 3/8" LOCKING PAN HEAD SCREW (10 PLCS)
NO. 6-32 x 3/8" PAN HEAD SCREW WITH INT. TOOTH LOCK WASHER (12 PLCS)
7
3
(REF) FREQUENCY BD (P/N 1100-00-0949)
NO. 6-32 x 3/8", 100° FLAT HEAD SCREW (6 PLCS)
NO. 6-32 x 5/8", 100° FLAT HEAD SCREW (6 PLCS)
(6) 14

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN F. FER	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL 11	PROTRACT		TITLE ASSEMBLY CHASSIS
FINISH WAVETEK PROCESS	RELEASE APPRV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0102-00-0812 REV F
	SCALE —	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-0812	WVTK	0102-00-0812	1
18	CABLE	178-0873	WVTK	1207-00-0873	1
3	SPRING REF 3200-01-0001	147-383	WVTK	1400-00-3750	1
19	MTG BKT	172-6332	WVTK	1400-00-6332	2
2	SHIELD PLATE	178-1203	WVTK	1400-01-1203	1
4	COVER, TOP	178-1222	WVTK	1400-01-1222	1
5	POWER ROD	178-1231	WVTK	1400-01-1231	1
6	BRKT, SHIELD MNTG	178-1683	WVTK	1400-01-1683	1
7	COVER, BOTTOM	178-3102	WVTK	1400-01-3102	1
20	SPRING GUARD-178	134-7980	WVTK	1400-01-7980	1
NONE	CHASSIS WELDMENT MODEL 178	178-1712	WVTK	1400-02-1712	1
8	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
9	CLAMP, CABLE	E-4	RICH	2800-00-0022	1
10	FLAT CABLE CLIP	FCA-15	WEKSR	2800-00-0027	9
17	SPACER .750H, .250 HEX6-32 THRU	2323	SMITH	2800-03-0010	7

WAVETEK PARTS LIST | TITLE: CHASSIS | ASSEMBLY NO. 1101-00-0812 | REV J

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
12	SPACER, NYLON .187 H, .375 DIA .194 THRU	13SP162	MROPL	2800-04-0013	9
13	BAIL W/FEET, 15 1/2	MP40008-5	BUKEY	2800-08-0001	1
14	NUT, SPEED, SELF RETAIN	C7494-632-4	TINN	2800-09-0003	6
21	SCREW, PAN CAD I WITH LONGLOK	6-32X3/8 PAN LL	CMRCL	2800-23-6106	10
16	SCREW, INSULATOR (NYLON)	10SC006015	MROPL	2800-28-0011	9

WAVETEK PARTS LIST | TITLE: CHASSIS | ASSEMBLY NO. 1101-00-0812 | REV J

PAGE 2

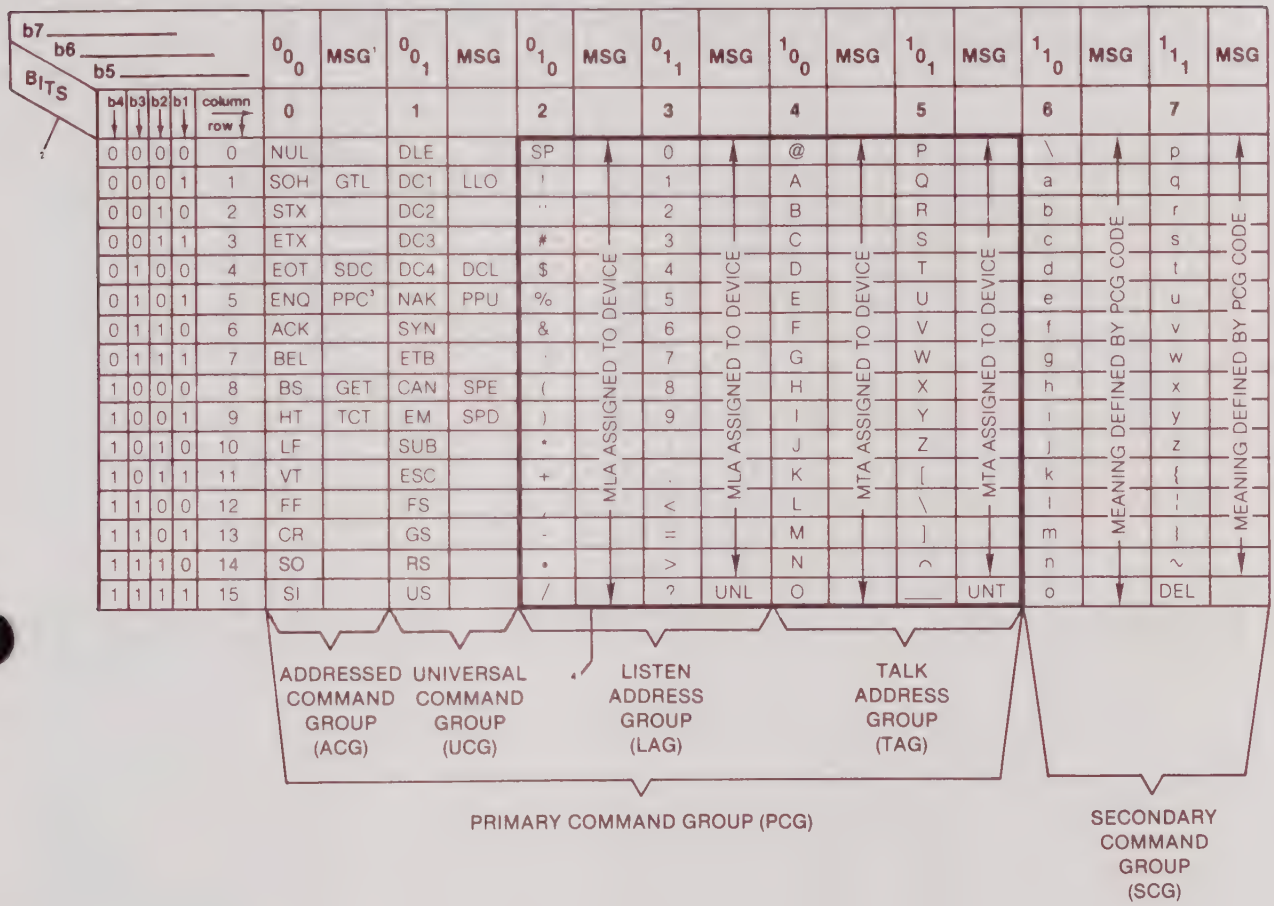
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 1101-00-0812 / REV J
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

APPENDIX A

American Standard Code for Information Interchange (ASCII)



b4	b3	b2	b1	col	row	0_0	MSG[1]	0_1	MSG	1_0	MSG	1_1	MSG	2_0	MSG	2_1	MSG	3_0	MSG	3_1	MSG
				0		NUL		DLE		SP		0		@		P		\		p	
0	0	0	1	1		SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2		STX		DC2		"		2		B		R		b		r	
0	0	1	1	3		ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4		EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5		ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6		ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7		BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8		BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9		HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10		LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11		VT		ESC		+		;		K		[		k		{	
1	1	0	0	12		FF		FS		,		<		L		\		l		|	
1	1	0	1	13		CR		GS		-		=		M		]		m		}	
1	1	1	0	14		SO		RS		.		>		N		^		n		~	
1	1	1	1	15		SI		US		/		?	UNL	O		_	UNT	o		DEL	

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	= DCL	Device clear	Universal Command Group
DC1	= LLO	Local lockout	
NAK	= PPU	Parallel poll unconfigure	
EM	= SPD	Serial poll disable	
CAN	= SPE	Serial poll enable	
SOH	= GTL	Go to local	Addressed Command Group
EOT	= SDC	Selected device clear	
ENQ	= PPC	Parallel poll configure	
BS	= GET	Group execute trigger	
HT	= TCT	Take control	

APPENDIX B

PROGRAMMING COMMAND SUMMARY
(Excluding GPIB Command Groups Given in Appendix A)

Control and Data Names	Model 178 Key	ASCII Character
Change Signs	+/–	–
Decimal Point	•	•
0, 1, 2, . . . 9	0, 1, 2, . . . 9	0, 1, 2, . . . 9
Amplitude	AMPL	A
Mode (Main)	MODE	B
Function	FUNC	C
Offset	OFFSET	D
Frequency	FREQ	F
Trigger Select (Ext/Int)	EXT/INT	G
Manual Trigger Released (Gate Off)	MAN TRIG (Released)	H
Execute	EXEC	I
Manual Trigger Pushed	MAN TRIG (Pressed)	J
Set Phase	PHASE	K
Set Phase Zero Reference	PHASE REF	L
Store Setting	STORE	M
Sweep Start Frequency	START FREQ	N
Sweep Stop Frequency	STOP FREQ	O
Output On or Off	ON/OFF	P
Trigger on Rising/Falling	SLOPE	Q
Burst Count	BURST	R
Sweep Mode	MODE	S
Sweep Time	TIME	T
Previous Stored Setting	_____	U
Vp-p, Vrms, VdBm Select	AMPL DEF	V
Next Stored Setting	_____	W
Recall Stored Setting	RECALL	Y
System Reset	RESET	Z
GET Mode	_____	XG
Frequency Sweep Hold	HOLD	XH
Frequency Sweep Resume	RESUME	XJ
Marker Select	MARKER	XN
Marker Frequency	MARKER FREQ	XO
Front or Rear Panel Output Select	FRONT/REAR	XP
SRQ Enable	_____	XQ
Talk Message	_____	XT
Terminator	_____	XV

APPENDIX B (Cont)

Function (C) Code

0 Sine
1 Triangle
2 Square
3 Ramp
4 DC
5 AM (Sine)

Main Generator Mode (B) Code

0 Continuous
1 Triggered
2 Gated
3 Burst
4 Triggered Haverwave
5 Gated Haverwave
6 Burst Haverwave

Sweep Mode (S) Code

0 Sweep Off
1 Continuous Sweep, Linear
2 Triggered Sweep, Linear
3 Triggered Sweep and Hold, Linear
4 Continuous Sweep, Logarithmic
5 Triggered Sweep, Lorarithmic
6 Triggered Sweep and Hold, Logarithmic

Output On/Off (P) Code

0 Output Off, Load Out
1 Output On
2 Output Off, 50Ω Load In

Front/Rear (XP) Code

0 Front Panel Output
1 Rear Panel Output

External/Internal Trigger (G) Code

0 Main Generator Triggered by External Input
1 Main Generator Triggered by Internal Generator

Trigger Slope (Q) Code

0 Rising Edge, Gate on High
1 Falling Edge, Gate on Zero

GET Mode (XG) Codes

NOTE: This parameter selects which kind of action the 178 will take when it receives a GET command.

0 Execute and trigger upon receipt of GET command (no error checking).
1 Fetch next stored setting, execute and trigger upon receipt of GET command (no error checking).
−1 Fetch previous stored setting, execute and trigger upon receipt of GET Command (no error checking).

SRQ (XQ) Code

NOTE: This parameter selects the conditions under which the GPIB flag is sent by the 178.

0 SRQ off.
1 SRQ sent if a programming error occurred.

Amplitude Definition (V) Code

0 Volt Peak-to-Peak
1 Volt rms
2 Volt dBm

Talk Message (XT) Code

NOTE: This parameter selects the kind of message the 178 will send when it is addressed as a talker on the GPIB.

0 Sweep Status. When read: 0 - No Sweep. 1 - Sweeping.
1 List of Programming Errors. When read, message sets to null.
2 Serial Poll byte message.
3 Value of most recently programmed selector.
4 Main Generator Settings.
5 Sweep Generator Settings.
6 Current Markers Frequency.
7 Model and Software Version.

APPENDIX C
DISPLAYS

Key Pressed	Display—ACTUAL (Explanation)
ADRS	GPIB ADDR (Decimal address) (Listen character) (Talk character)
AMPL	AMPL (Value) (Unit of measure Vp-p, Vrms, dBm)
AMPL DEF	AMPL IN (Unit of measure selected Vp-p[0], Vrms[1], dBm[2])
♪ (beep)	(Audible beep)
BURST	BURST COUNT (Value)
CLEAR ENTRY	(Clears any unexecuted numerical entry of the last parameter entered)
CMD RCL	(A string of letters and numbers up to 40 characters long displayed 20 characters at a time and shifted by the cursor →, ←)
CURSOR ←, →	(If a value is being displayed, the selected digit blinks. If there is no value being displayed, there is no effect. If it was a command recall or type 2 error display, ← shifts the display 4 characters to the left. If it was a command recall or type 2 error display, → shifts the display 4 caracters to the right.)
CURSOR ↑	(If the display is a value, code or storage location number, it increments.)
CURSOR ↓	(If the display is a value, code or a storage location number, it decrements.)
DISPLAY TEST	(All display segments are lit.)
EXEC	If no errors: EXECUTE. If class 1 error: (Parameter identified) ERROR. If class 2 error: ERROR (Parameter identified).
EXP	(If previous display was a value or a code, it is suffixed with an E0.)
EXT/INT	(INTERNAL or EXTERNAL) TRIGGER (Code)
FRONT/REAR	(FRONT or REAR) OUTPUT (Code)
FREQ	FREQ (Value) (μHz, mHz, Hz, kHz or MHz)
FUNC	FUNC (Function) (Code)
HOLD	HOLD AT (Value) (μHz, mHz, Hz, kHz or MHz)
LOCAL	(No change)
MAN TRIG	(When pressed: No display if in continuous mode, TRIGGER if in any triggered or burst mode, GATE if in gated mode, and when released, no effect in any triggered, gate, or burst mode.
MODE (Main)	MODE (CONTINUOUS [0] TRIGGERED [1], GATED [2], BURST [3], TRIG HAVER [4], GATED HAVER [5] BURST HAVER [6])

Key Pressed	Display—ACTUAL (Explanation of Possible Displays)
MODE (Sweep)	SWP (OFF [0], CONT LIN [1], TRIG RST LIN [2], TRIG HOLD LIN [3], CONT LOG [4], TRIG RST LOG [5], or TRIG HOLD LOG [6])
MARKER	MARKER (Number) (Frequency) (μHz, mHz, Hz, kHz or MHz)
MARKER FREQ	MKR FRQ (Value) (μHz, mHz, Hz, kHz or MHz)
OFF/ON	OUTPUT (OFF, LD OUT (0) or OFF, LD IN (2)
OFFSET	OFFSET (Value) (μV, mV or V)
PHASE REF	PHASE REFERENCE SET
PHASE	PHASE (Value) DEG or NO PHASE (SWEEPING)
RESUME	RESUME
RECALL	SETTING (Value) RECALLED
RESET	RESET
SLOPE	TRIG SLOPE (POS [0] or NEG [1])
START FREQ	SW STRT (Value) (μHZ, mHZ, HZ, kHZ or MHZ)
STOP FREQ	SW STOP (Value) (μHZ, mHZ, HZ, kHZ or MHZ)
STORE	If no errors: NO. (Value) LAST STORED. If class 1 error: (Parameter identified) ERROR. If class 2 error: (Parameter identified).
STATUS	Display changes automatically: FREQ (Value) (μHZ, mHZ, kHz or MHZ) AMPL (Value) Unit of measure Vp-p, Vrms, dBm) OFFSET (Value) (μV, mV or V) FUNC (Function) (Code) MODE (Main generator mode) (Code) BURST COUNT (Value) PHASE (Value) DEG SW STRT (Value) (μHZ, MHZ, kHZ or MHZ) SW STOP (Value) (μHZ, mHZ, HZ, kHZ or MHZ) MKR FRQ (Value) (μHZ, mHZ, HZ, kHZ or MHZ) SELECTED SWP (Mode) (Code) SWEEP TIME (Value) SEC OUTPUT (ON or OFF) (Code) (FRONT or REAR) OUTPUT (Code) (EXTERNAL or INTERNAL) TRIGGER (Code) TRIG SLOPE (POS or NEG) (Code)
TIME	SWEEP TIME (Value) SEC
(Number Keys)	(Number corresponding to the selected key)

Under remote operation, certain characters may appear in the extreme right side of the display. Those characters are:

R — Remote

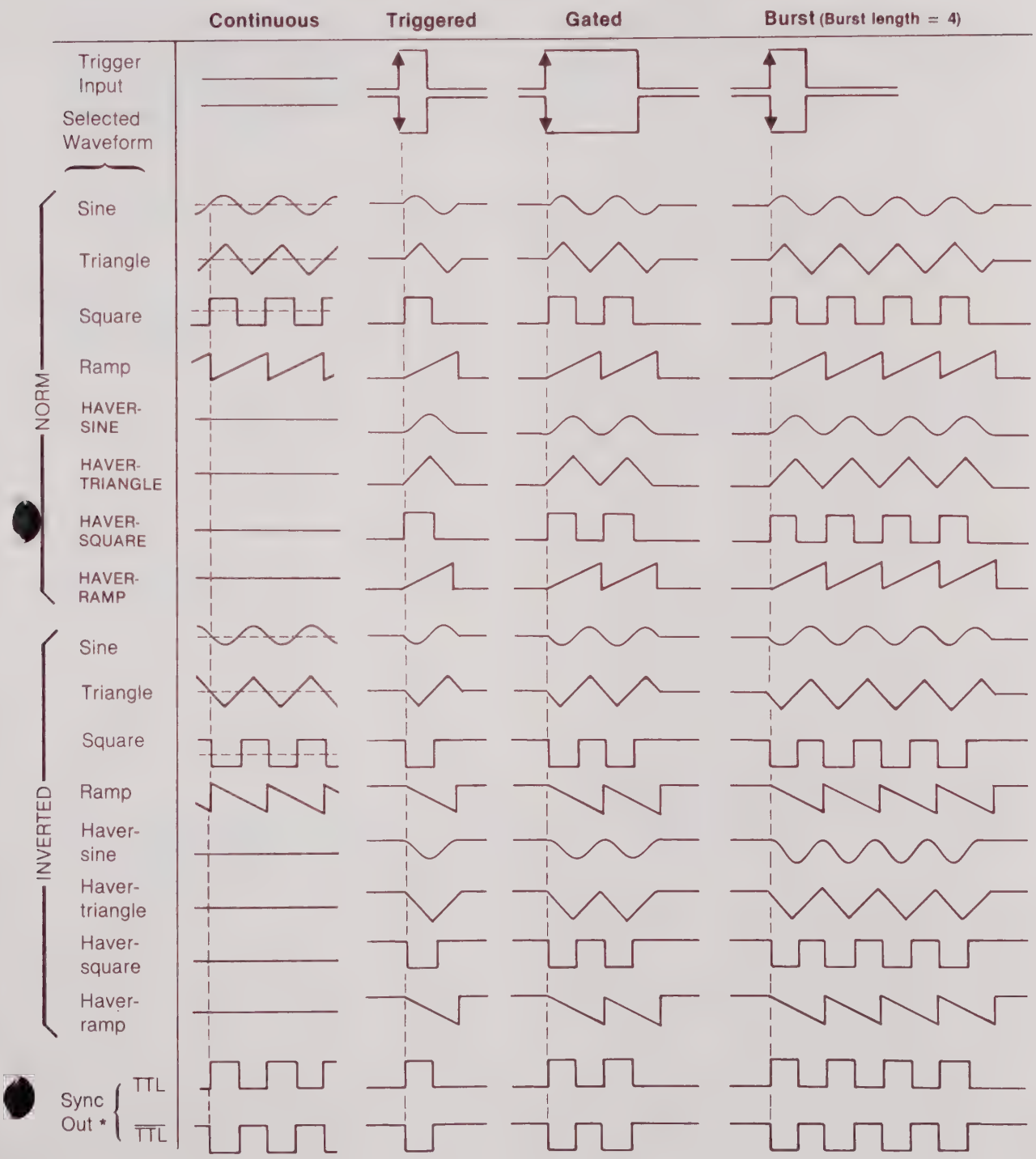
L — Addressed to Listen

T — Addressed to Talk

Q — Request for service because of either Class 1 or Class 2 errors.

APPENDIX D

OUTPUT AND TIMING FOR BASIC MODES AND FUNCTIONS



*In phase with square wave only.

APPENDIX E
MODE COMBINATIONS AND OUTPUT

With seven main generator modes, seven sweep generator modes and two trigger modes, the number of possible output configurations is very large; however, as can be seen from table 3-5, it is sufficient to illustrate only 28 of these configurations and to extrapolate for the remainder.

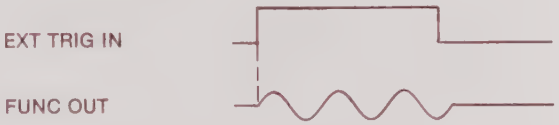
NOTE
SWEEP OFF refers to the state of the main generator not the sweep generator.

B0,S0 (Main Cont, Sweep Off)—A continuous fixed frequency is supplied by the main generator. Sweep output, a continuous ramp, is unrelated to the function output.

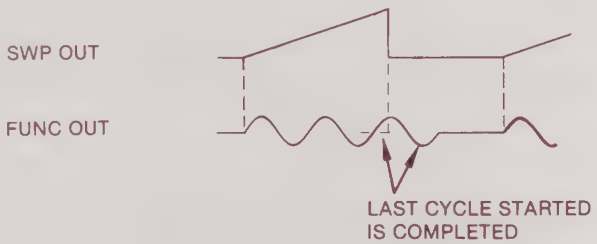
B1,S0,G0 (Main Triggered, Sweep Off, Main Triggered Externally)—A trigger initiates a single cycle at the selected frequency.

B1,S0,G1 (Main Triggered, Sweep Off, Main Triggered by Sweep)—The sweep generator triggers the main generator producing a single cycle at the selected frequency.

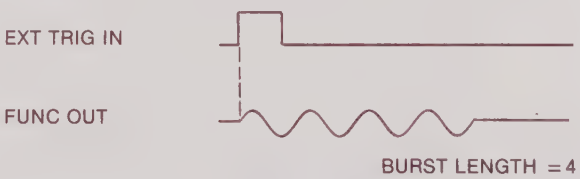
B2,S0,G0 (Main Gated, Sweep Off, Main Gated Externally)—The main generator is gated on for a period determined by the trigger input at a fixed frequency.



B2,S0,G1 (Main Gated, Sweep Off, Main Gated by Sweep)—The main generator is gated by the sweep generator with the gate time dependent upon the sweep time.

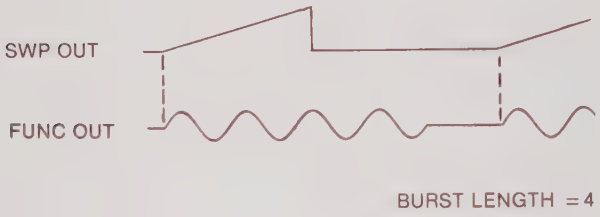


B3,S0,G0 (Main Burst, Sweep Off, Main Externally Triggered)—A trigger initiates a fixed frequency burst at the selected frequency for a period determined by the burst length.

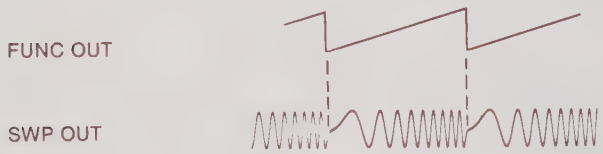


APPENDIX E (Cont)

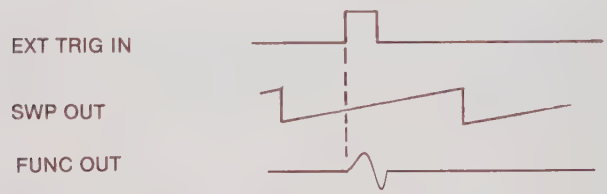
B3,S0,G1 (Main Burst, Sweep Off, Main Triggered by Sweep)—The sweep generator triggers a fixed frequency burst from the main generator at the selected frequency for the duration of the programmed burst length.



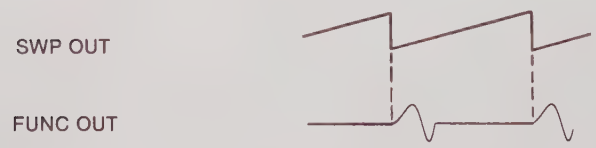
B0,S1 (Main Cont, Sweep Cont)—The output is a continuous output continuously sweeping from the start to the stop frequency.



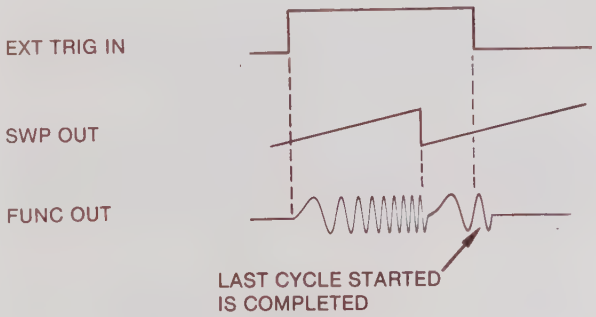
B1,S1,G0 (Main Triggered, Sweep Cont, Main Triggered Externally)—A single cycle of a sweeping waveform is generated for each trigger.



B1,S1,G1 (Main Triggered, Sweep Cont, Main Triggered by Sweep)—The sweep generator triggers a single cycle at the start frequency.

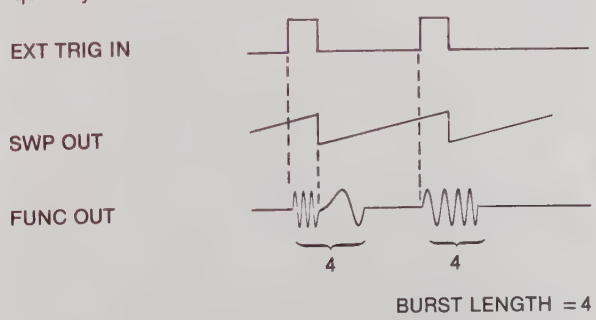


B2,S1,G0 (Main Gated, Sweep Cont, Main Gated Externally)—When the trigger signal is received the main generator produces a sweep burst proportional to the trigger pulse width. The start frequency is random, somewhere between the start and stop frequency.



B2,S1,G1 (Main Gated, Sweep Cont, Main Gated by Sweep)—The sweep generator triggers the main generator producing a sweep burst whose frequency varies between the start and stop frequency for a period set by the sweep time.

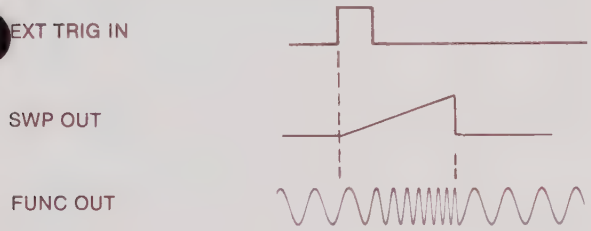
B3,S1,G0 (Main Burst, Sweep Cont, Main Triggered Externally)—When triggered, the main generator outputs a sweep burst for a period determined by the burst length. The beginning frequency is random, somewhere between the start and stop frequency.



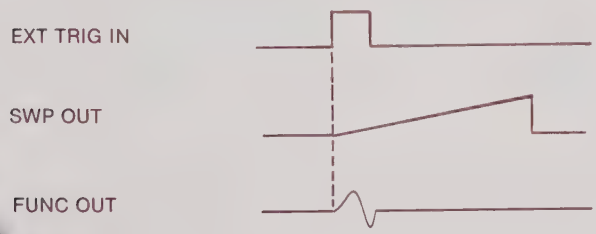
APPENDIX E (Cont)

B3,S1,G1 (Main Burst, Sweep Cont, Main Triggered by Sweep)—The sweep generator initiates a sweep burst beginning at the start frequency and ending after a specific number of cycles which is determined by the burst length.

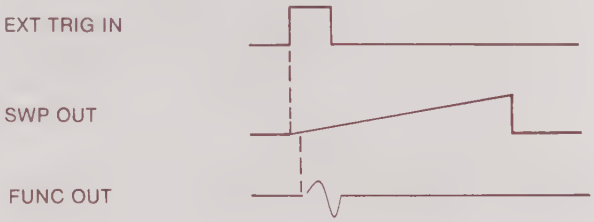
B0,S2 (Main Cont, Sweep Triggered Externally)—The main generator runs continuously at the start frequency, when an external trigger is received the main generator sweeps from the start to the stop frequency and resets to the start frequency.



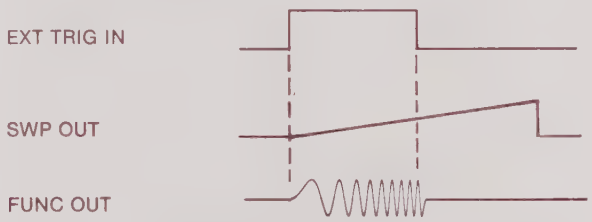
B1,S2,G0 (Main Triggered, Sweep Triggered, Main Triggered Externally)—An external pulse triggers the main and sweep generators, which produces a single sweeping cycle near the start frequency.



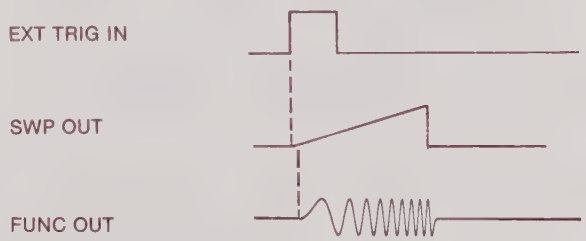
B1,S2,G1 (Main Triggered, Sweep Triggered Externally, Main Triggered by Sweep)—External trigger triggers the sweep generator, which triggers the main generator to generate a single nonsymmetrical cycle as in external trigger.



B2,S2,G0 (Main Gated, Sweep Triggered Externally, Main Gated Externally)—A trigger input gates the main generator tus producing a gated sweep from the start freuqency with the trigger duration determining the burst length.

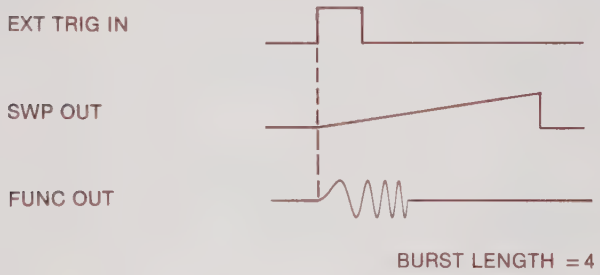


B2,S2,G1 (Main Gated, Sweep Triggered Externally, Main Gated by Sweep)—The sweep generator is triggered which gates and sweeps the main generator for the duration of the sweep time.

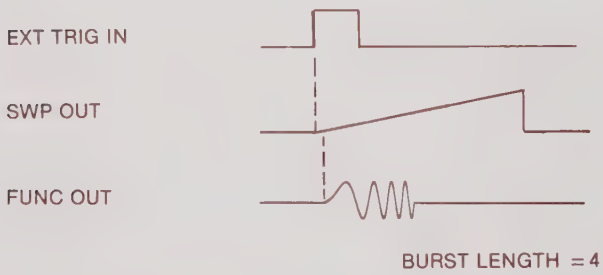


APPENDIX E (Cont)

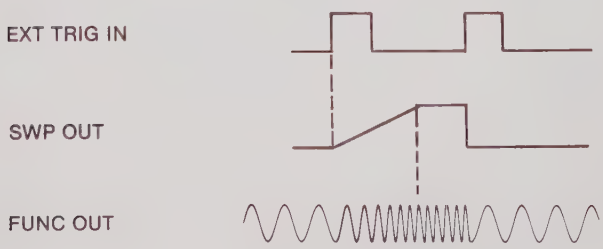
B3,S2,G0 (Main Burst, Sweep Time Externally, Main Triggered Externally)—External trigger triggers a sweep burst from the main generator. Burst duration is set by the burst length.



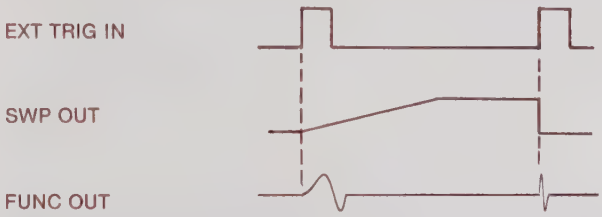
B3,S2,G1 (Main Burst, Sweep Triggered, Main Triggered by Sweep)—The sweep generator, triggered by an external trigger, triggers the main generator. The burst duration is set by the burst length.



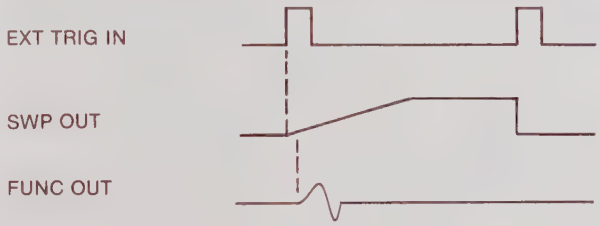
B0,S3 (Main Cont, Triggered, Reset Sweep)—The main generator runs continuously at the start frequency. When triggered, the main generator sweeps to the stop frequency and holds. a second trigger resets the main generator from the stop to start frequency.



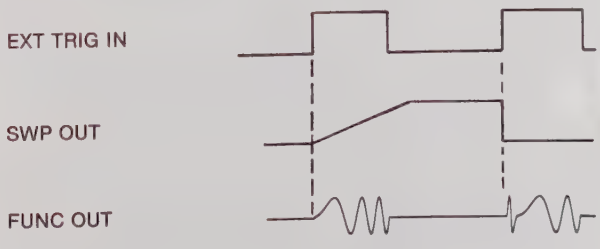
B1,S3,G0 (Main Triggered, Triggered Sweep/Triggered Sweep Reset Externally, Main Triggered Externally)—An external trigger simultaneously triggers the main and sweep generators that generates a single nonsymmetrical cycle at the start frequency. A second trigger resets the generator to the start frequency and triggers the main geneartor producing a single nonsymmetrical cycle at the stop frequency.



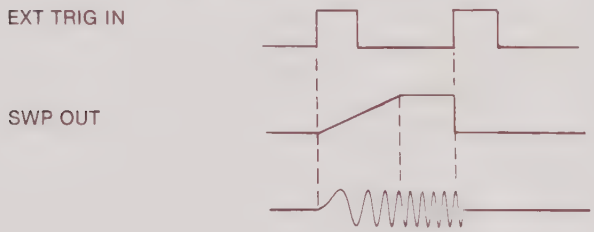
B1,S3,G1 (Main Triggered, Triggered Sweep/Triggered Sweep Reset Externally, Main Triggered by Sweep)—Is identical to external trigger except the second trigger will not trigger the main generator.



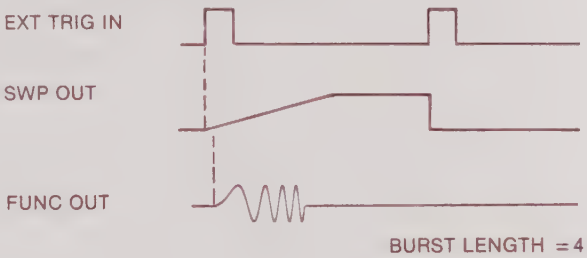
B2,S3,G0 (Main Gated, Triggered Sweep/Triggered Reset Externally, Main Gated Externally)—The trigger initiates a sweep burst beginning at the start frequency and ending at a period dependent upon the trigger pulse period. A second trigger resets the sweep generator and gates the main generator which again sweeps for the duration of the trigger pulse width.



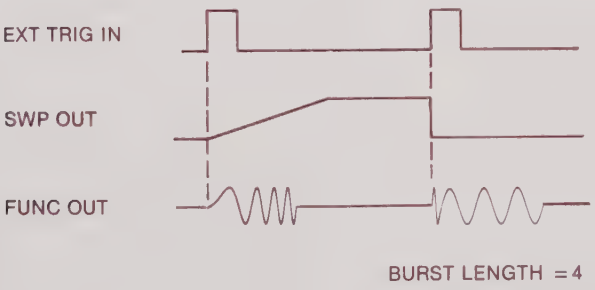
B2,S3,G1 (Main Gated, Triggered Sweep/Triggered Reset Externally, Main Gated by Sweep)—The main generator is gated by the triggered sweep generator. The sweep burst sweeps from the start frequency to the stop frequency with burst duration determined by sweep time. A second trigger resets the sweep generator to the start frequency without triggering the main generator.



B3,S3,G1 (Main Burst, Triggered Sweep/Triggered Reset Externally, Main Triggered by Sweep)—A sweep burst of the main generator is started by an externally triggered sweep generator. The burst sweeps from the start frequency for a period set by the burst length. A second triggers the sweep generator without triggering the main generator.



B3,S3,G0 (Main Burst, Triggered Sweep/Triggered Sweep Reset Externally, Main Triggered Externally)—The sweep and main generators are simultaneously triggered, which initiates a sweep burst beginning at the start frequency for a duration dependent upon the programmed burst length. A second trigger resets the sweep generator also triggering the main generator also triggering the main generator for the burst length.



APPENDIX F
OPTIONS 001 AND 002

Option 001: Stored Settings

Refer to paragraphs 1.2, 3.10 and 3.16.7 and the drawings and parts list following this page.

Option 002: High Stability Frequency Reference

Refer to paragraph 1.2, instrument schematic and reference board drawings/parts list in section 7.

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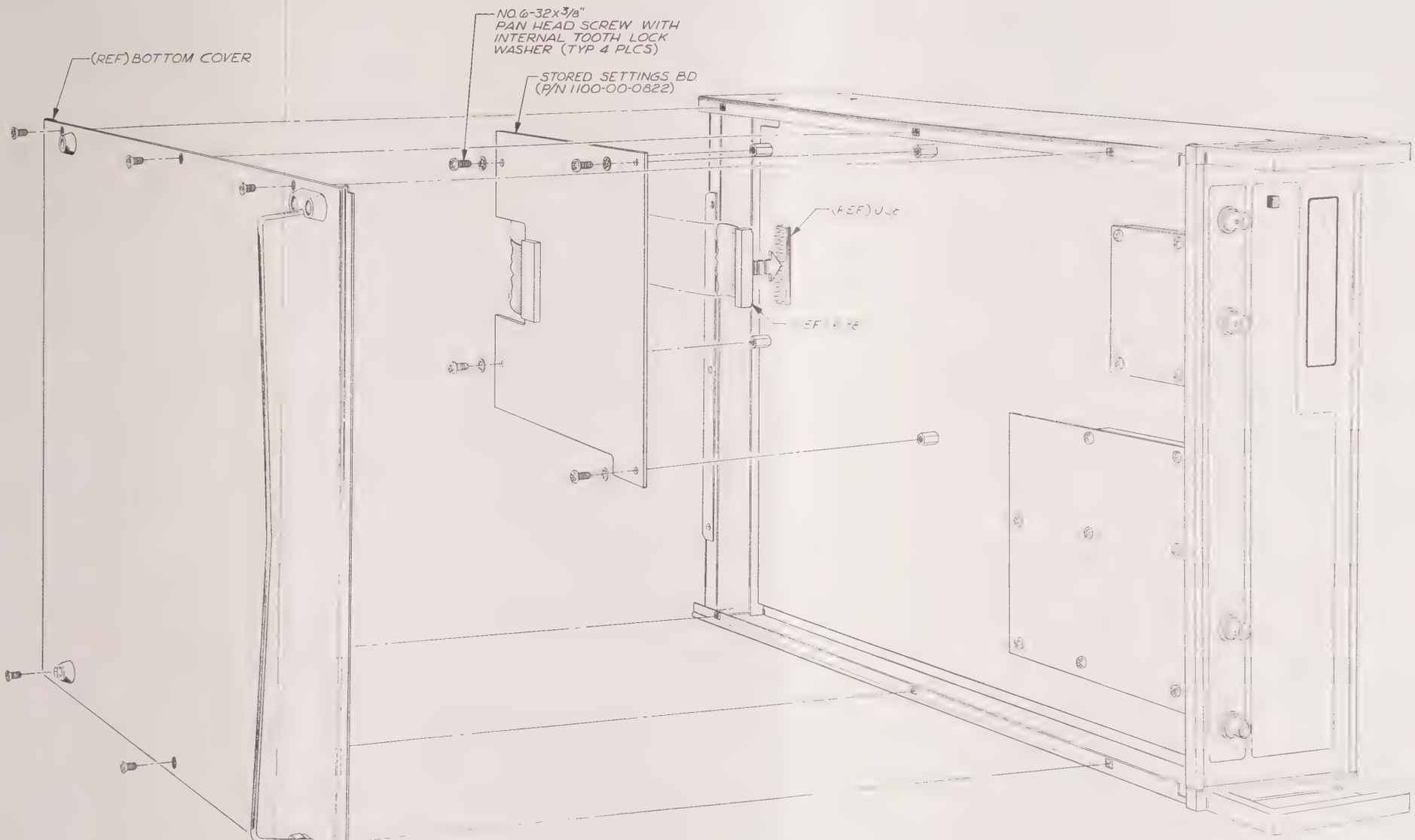
REV	ECN	BY	DATE	APP


(REF) BOTTOM COVER
NO.6-32x3/8" PAN HEAD SCREW WITH INTERNAL TOOTH LOCK WASHER (TYP 4 PLCS)
STORED SETTINGS BD. (P/N 1100-00-0822)
(REF) J38
(REF) P38

STORED SETTINGS BOARD INSTALLATION

CONNECT "P38" TO "J38" THEN INSTALL STORED SETTINGS BOARD WITH HARDWARE, AS SHOWN

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: INSTALLATION DRAWING STORED SETTINGS (001 OPTION)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 0002-00-0169 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3864

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REV	ECN	BY	DATE	APP
D	ECN 2527	LDU	1-15-81	
E	ECN 2742, 2745	DC	8/26/81	DC
/	3526 (CL II)	[illegible]	11/3/83	[illegible]
F	# 3923	SC	[illegible]	[illegible]
G	ECN 6006	RO	9/14/89	

J40 RIBBON CABLE

U3-13 … U3-11

LS245 U2 — R1 6.8K SIP — LS273 U1

BAD Ø … BAD 7 — BA Ø … BA 7

READ (A5) — BAS (D3) — +5V

LS368 U3

R2 10K, R3 10K

DB Ø — DB 7 — BR/W (B6) — BAS (D5) — BR/W (A6)

(B8) R/W — (C7) BA15 — (C8) AS

LS244 U4

BA8 — BA9 — BA10 — BA11 — BA12 — BA13 — BA14 — BA15 (D3)

E — AS (D3) — SS TEST — 20 MHz — R/W (D3) — +5V

HM6116-LP4 U8 — U9 — U10 — U11 — U12 — U13

BAD Ø … BAD 7

CS1 — CS2 — CS3 — CS4 — CS5 — CS6

R7 … R12 1K

CR1 MBR120 — +5V

R6 21.5 — B+ (A2, B5)

C1 D1/50V — BT1 3.6V

B+ (C1)

PIN #21 DESTINATION IS TYPICAL U8 THRU U15

+5V — WRP (B5)

R4 10K — 1/4 LS08 U6 — 1/3 7410 U7 — R15 1K — NRD (B1)

BE — BR/W (D3)

BA14 — BA15 — 1/4 LS08 U6 — 1/3 7410 U7 — R5 1K — READ (D6, B8)

BE — BR/W (D3)

1/3 7410 U7 — CS (A4)

B+

LS138 U5

BA11 — BA12 — BA13

CS1 … CS8

R16 10K — CR2 1N4002 — +5V — C19 100µf/16V

(A6) CS

FB1

C2 … C16 100/16V, 1/50V

1. ALL RESISTORS ARE IN OHMS
2. ALL CAPACITORS ARE IN µf
4. PARTIAL REFERENCE DESIGNATOR SHOWN, PREFIX WITH ASSEMBLY REF DES (A9)

⚠5 PIN DESTINATIONS WITHIN BRACKETS ON U8 ARE TYPICAL FOR U9, U10, U11, U12, U13, U14.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S CHERMACK	DATE 9-25-80	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC: STORED SETTINGS BD (A9)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 178	DWG NO 0103-00-0822 REV G
	SCALE	CODE IDENT 23338	SHEET / OF /

0103-00-0822

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3884

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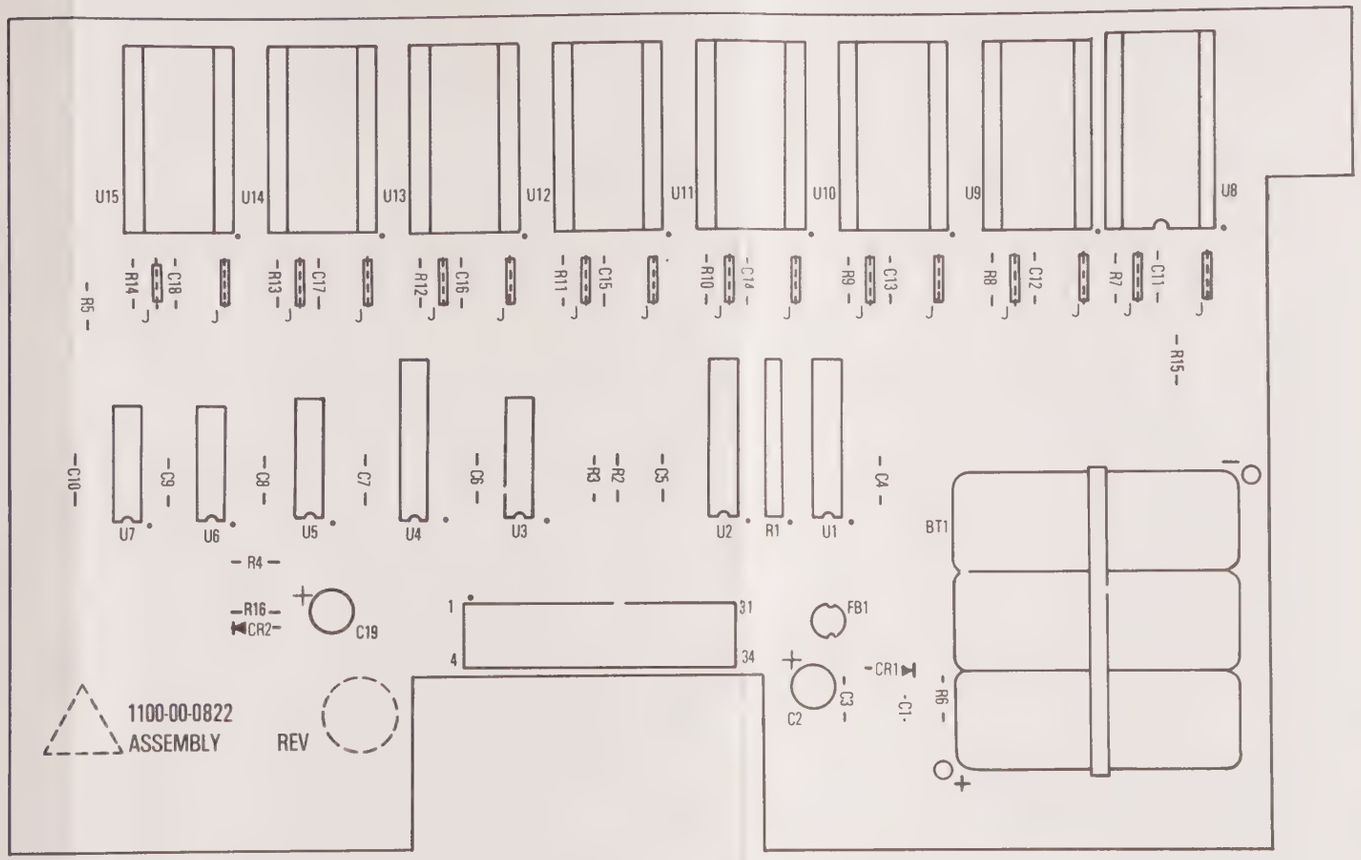

MADE FROM 0100-00-0822-3E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA STORED SETTINGS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 178 / DWG NO 1100-00-0822 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, STORED SETTINGS	0101-00-0822	WVTK	0101-00-0822	1
NONE	SCHEMATIC, STORED SETTINGS	0103-00-0822	WVTK	0103-00-0822	1
C1	CAP, CER, MN, .01MF, 50V	GE50-103ZA	MURAT	1500-01-0310	1
C10 C11 C12 C13 C14 C15 C16 C3 C4 C5 C6 C7 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	14
C2	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	1
C19	CAP, ELECT, 100MF/16V RADIAL LEAD, SP .20	CRE SERIES 100/16	CAPAR	1500-31-0111	1
NONE	PCB, STORED SETTINGS	178-0822	WVTK	1700-00-0822	1
NONE	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	6
FB1	BALUN CORE	2873000902	FARIT	3100-00-0002	1
BT1	BATTERY, 3.6V	KQ3B1/1AA-QT1	GE	4000-02-0006	1
R10 R11 R12 R15 R5 R7 R8 R9	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	8
R16 R2 R3 R4	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	4
R6	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	1
R1	RES MODULE	4310R-101-682	BOURN	4770-00-0016	1

WAVETEK PARTS LIST | TITLE: PCA, STORED SETTINGS | ASSEMBLY NO. 1100-00-0822 | REV E

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR2	DIODE	1N4002	FAIR	4801-02-0001	1
CR1	DIODE	MBR 120	MOT	4806-02-0120	1
J40	ASSY, RIBBON CABLE 34 PIN X 2.5 LONG	6002-00-0016	WVTK	6002-00-0016	1
U10 U11 U12 U13 U8 U9	CMOS, S-RAM, 2K x 8	HM6116LP-4	HTACH	8000-61-1600	6
U6	TTL, AND, QUAD 2INP	74LS08	TI	8000-74-0810	1
U7	IC	7410	TI	8000-74-1000	1
U5	TTL, DCDR, 3-8 LINE	74LS138	TI	8007-41-3810	1
U4	TTL, BUF, OCT, 3 ST OUT	74LS244	TI	8007-42-4410	1
U2	TTL, XCVR, OCT BUS	74LS245	TI	8007-42-4510	1
U1	TTL, D-F/F, OCT	74LS273	TI	8007-42-7310	1
U3	IC	74LS368	TI	8007-43-6810	1

WAVETEK PARTS LIST | TITLE: PCA, STORED SETTINGS | ASSEMBLY NO. 1100-00-0822 | REV E

PAGE 2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS

DRAWN | DATE | PROJ ENGR | RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ±.010 ANGLES ±1°
XX ±.030

DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST PCA, STORED SETTINGS

MODEL NO.	DWG NO.	REV
178	1100-00-0822	E

CODE IDENT 23338 | SHEET 1 OF 1

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